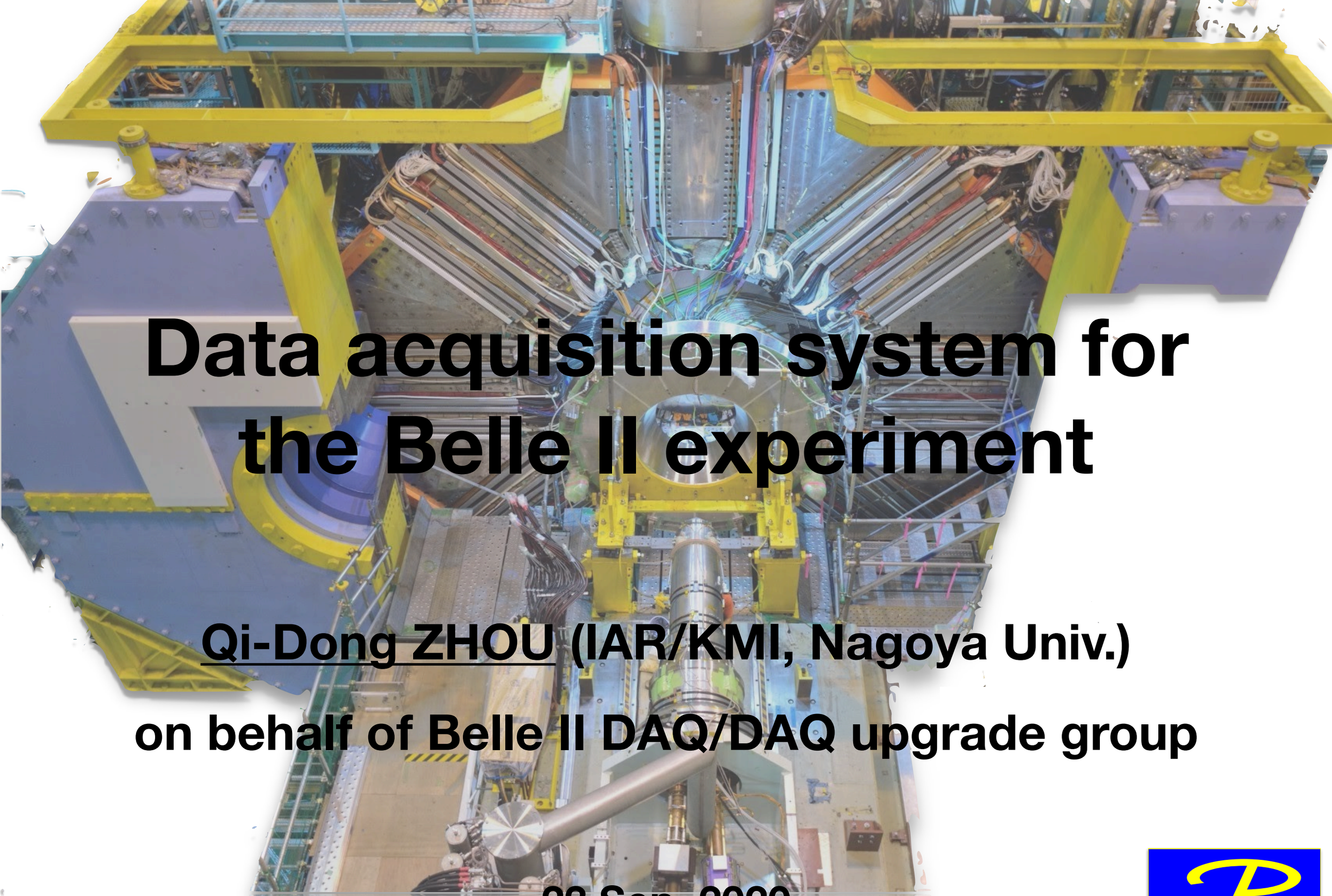


Data acquisition system for the Belle II experiment

Qi-Dong ZHOU (IAR/KMI, Nagoya Univ.)

on behalf of Belle II DAQ/DAQ upgrade group

23 Sep. 2020
KMI Topics

Contents

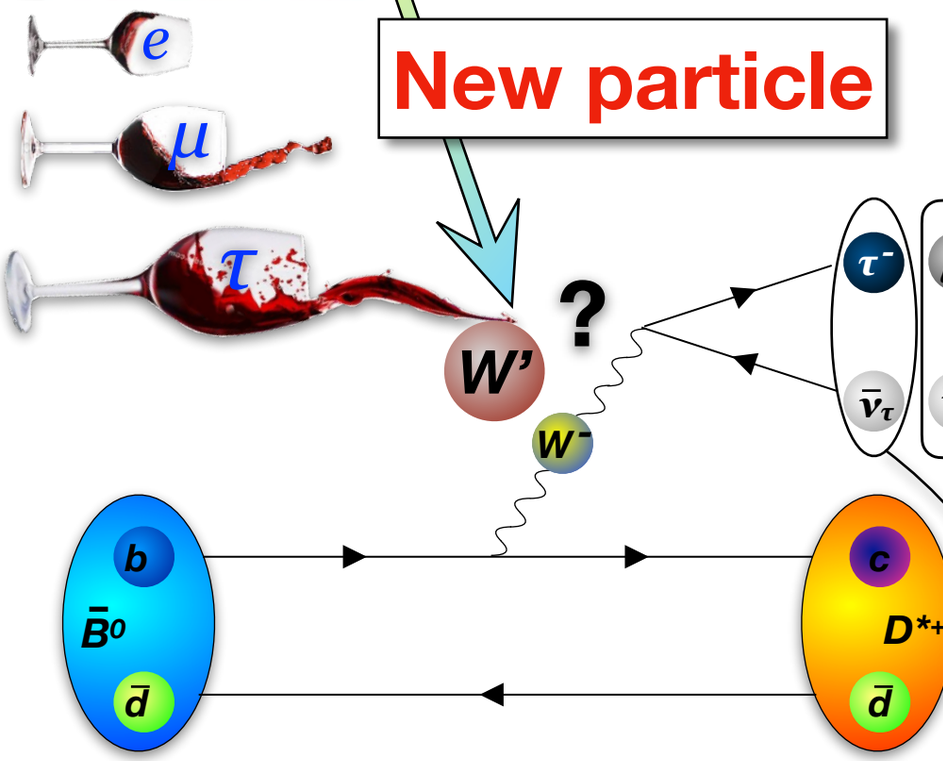
- SuperKEKB accelerator
- Belle II detector
- Belle II DAQ system
- DAQ performance in 2020 ab run
- Belle II DAQ upgrade
- Development status and performance of upgrade system
- Schedule and plan of DAQ upgrade

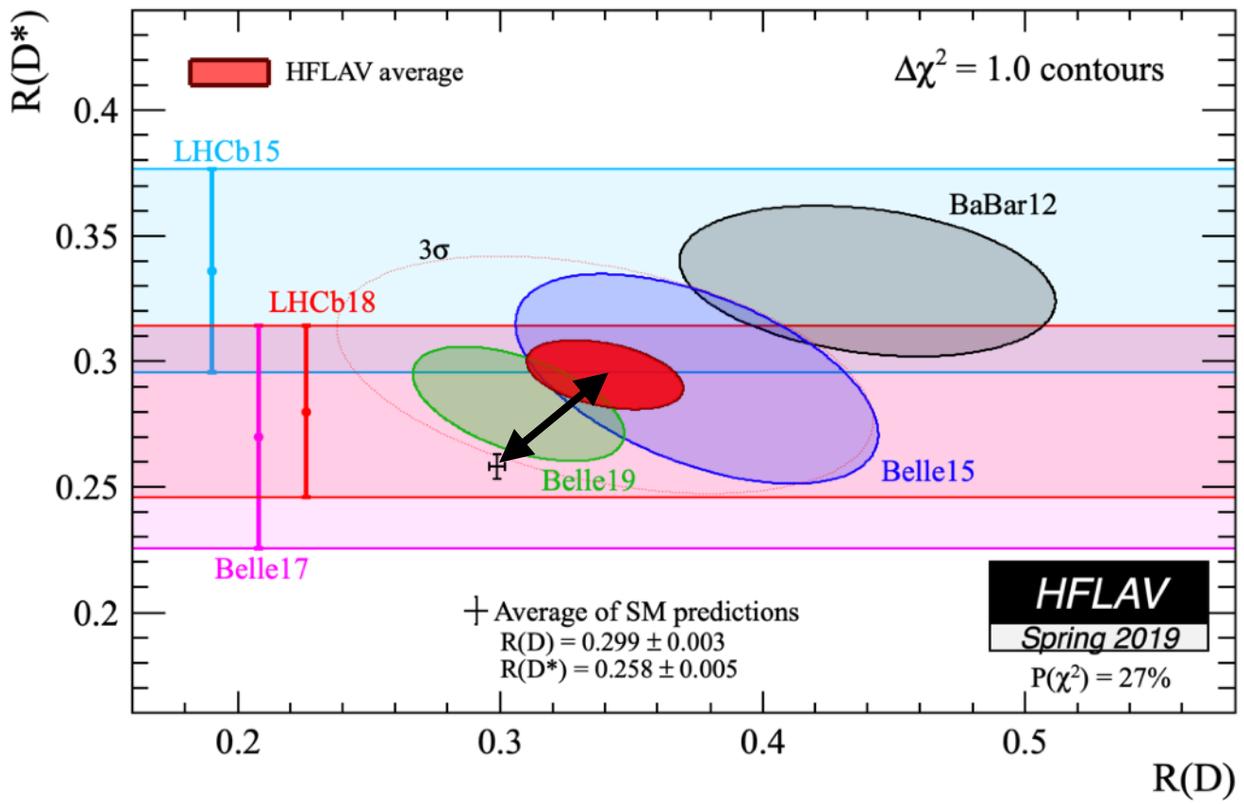
New physics search

Two approaches to explore NP

① **Energy frontier,**
Large Hadron Collider (LHC)

② **Luminosity frontier,**
SuperKEKB accelerator





$$\bar{B}^0 \to D^{*+}[W^- \to \tau^- \bar{\nu}_\tau]$$

$$R_{(D^*)} = \frac{Br(\bar{B}^0 \to D^{*+}\tau^- \bar{\nu}_\tau)}{Br(\bar{B}^0 \to D^{*+}\ell^- \bar{\nu}_\tau)}$$

Luminosity frontier: SuperKEKB

Beam current: KEKB x 1.7

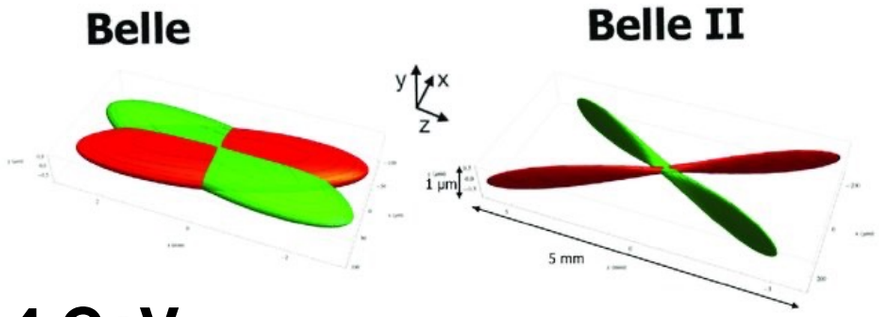
$\mathcal{L}$ = 6.5 x 10^{35} cm^{-2} s^{-1}

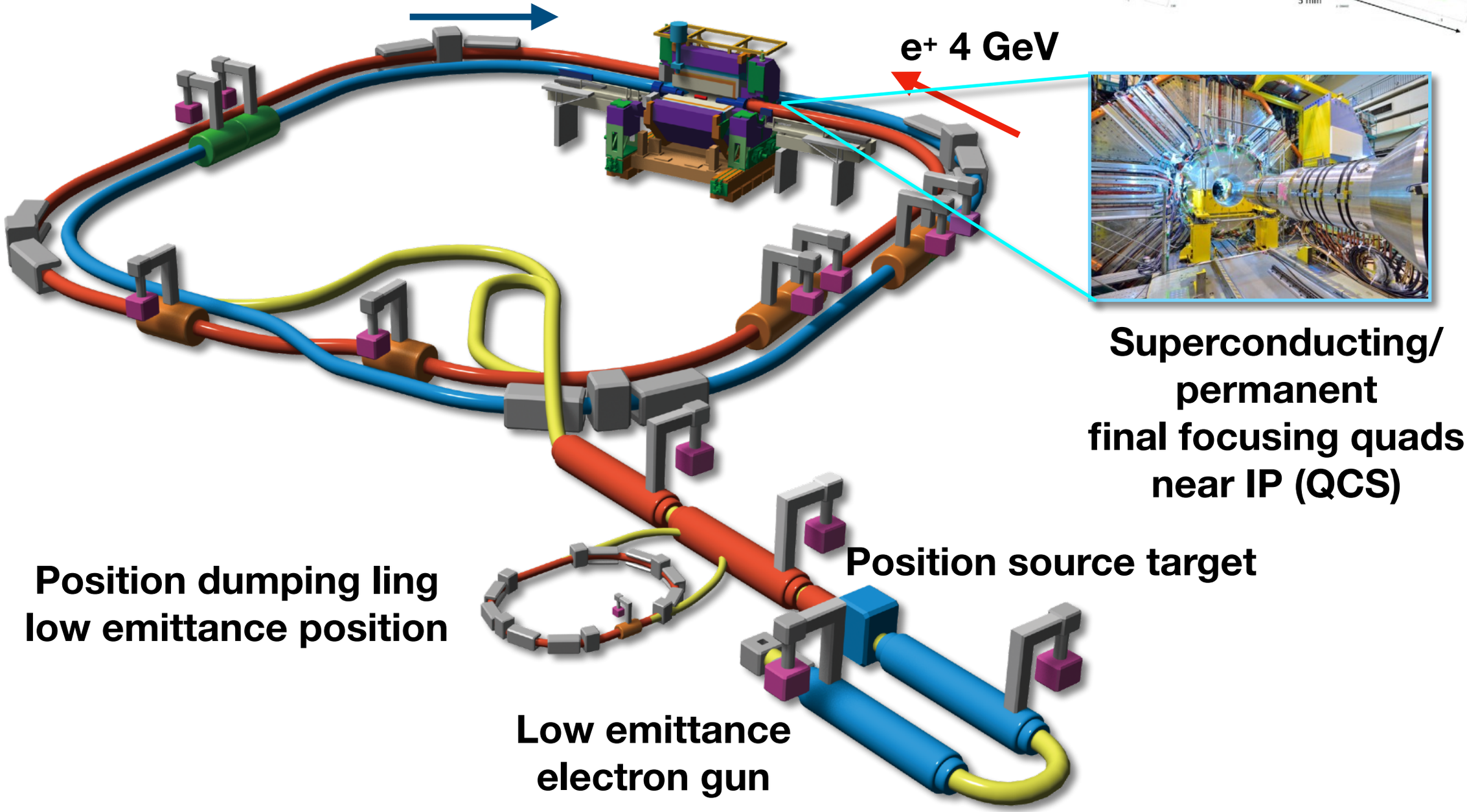
Luminosity

$$L = \frac{\gamma_{\pm}}{2er_e}\left(1+\frac{\sigma_y^*}{\sigma_x^*}\right)\frac{I_{\pm}\xi_{\pm y}}{\beta_y^*}\left(\frac{R_L}{R_y}\right)$$

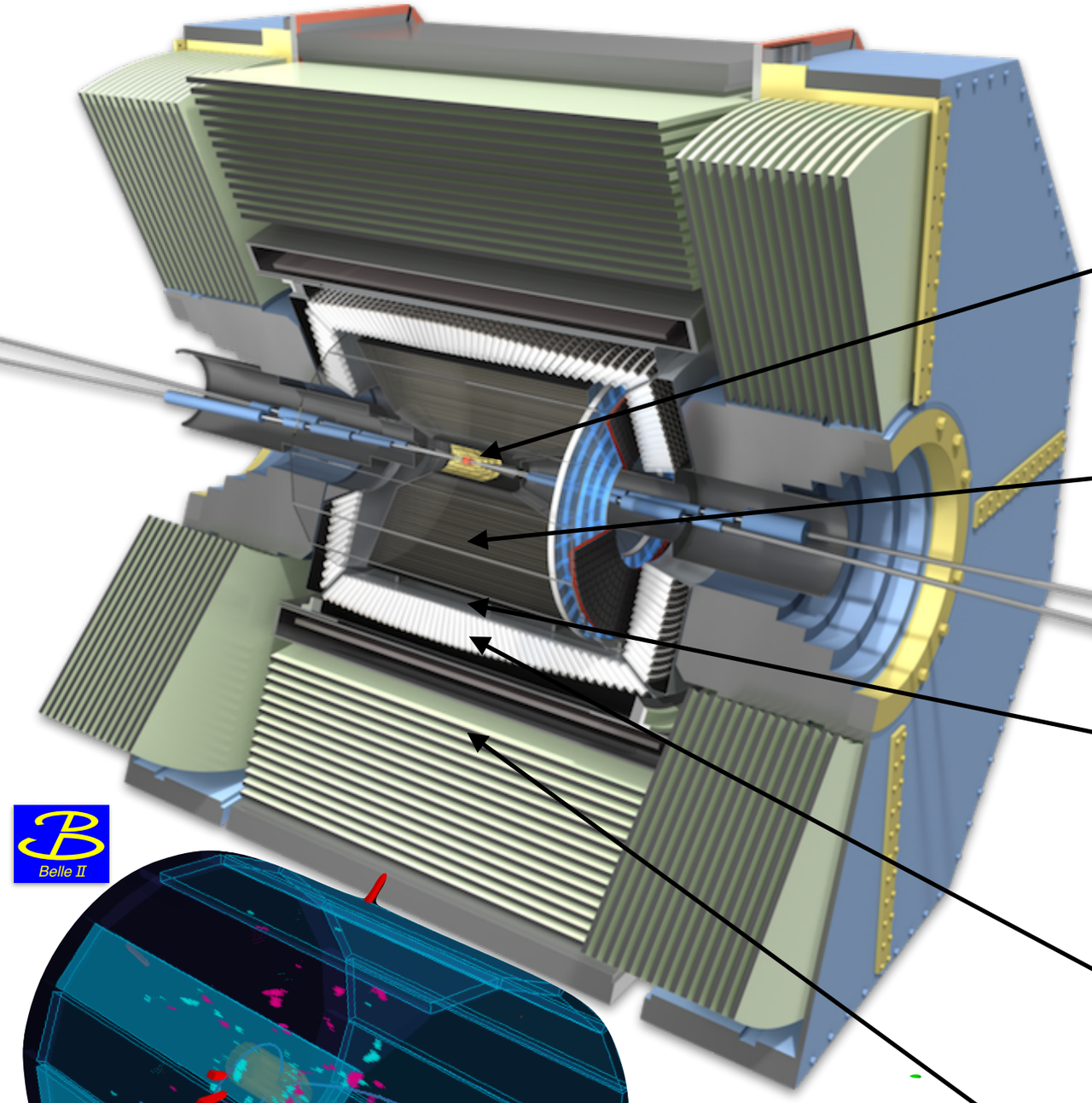
Beam squeeze: KEKB / 20

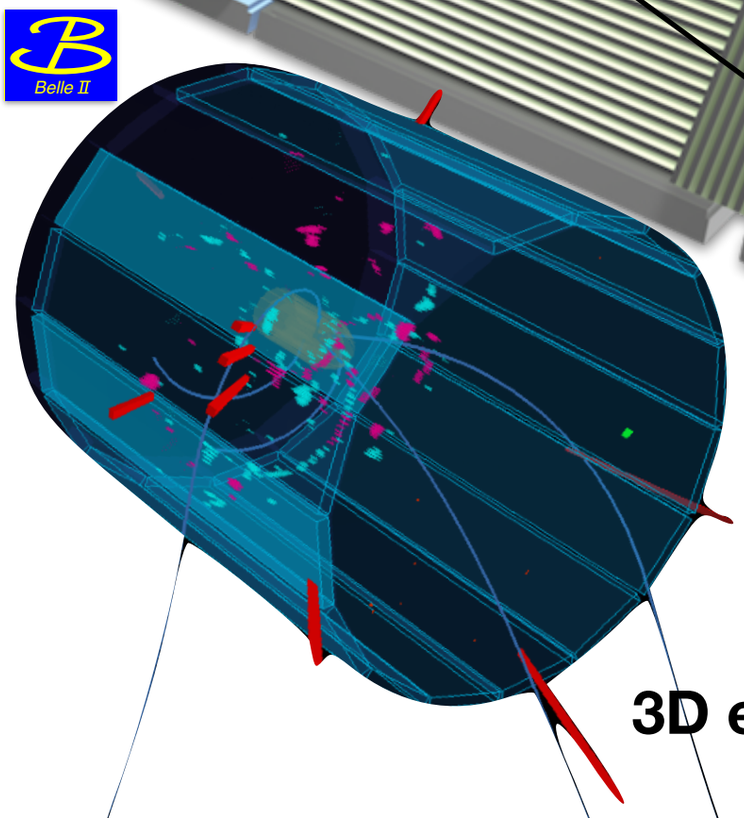
Nano beam scheme





Belle II detector





3D event display

Vertex detector (VXD)
- Inner 2 layers: pixel detector (PXD)
  - 2nd layer not fully installed
- Outer 4 layers: strip sensor (SVD)

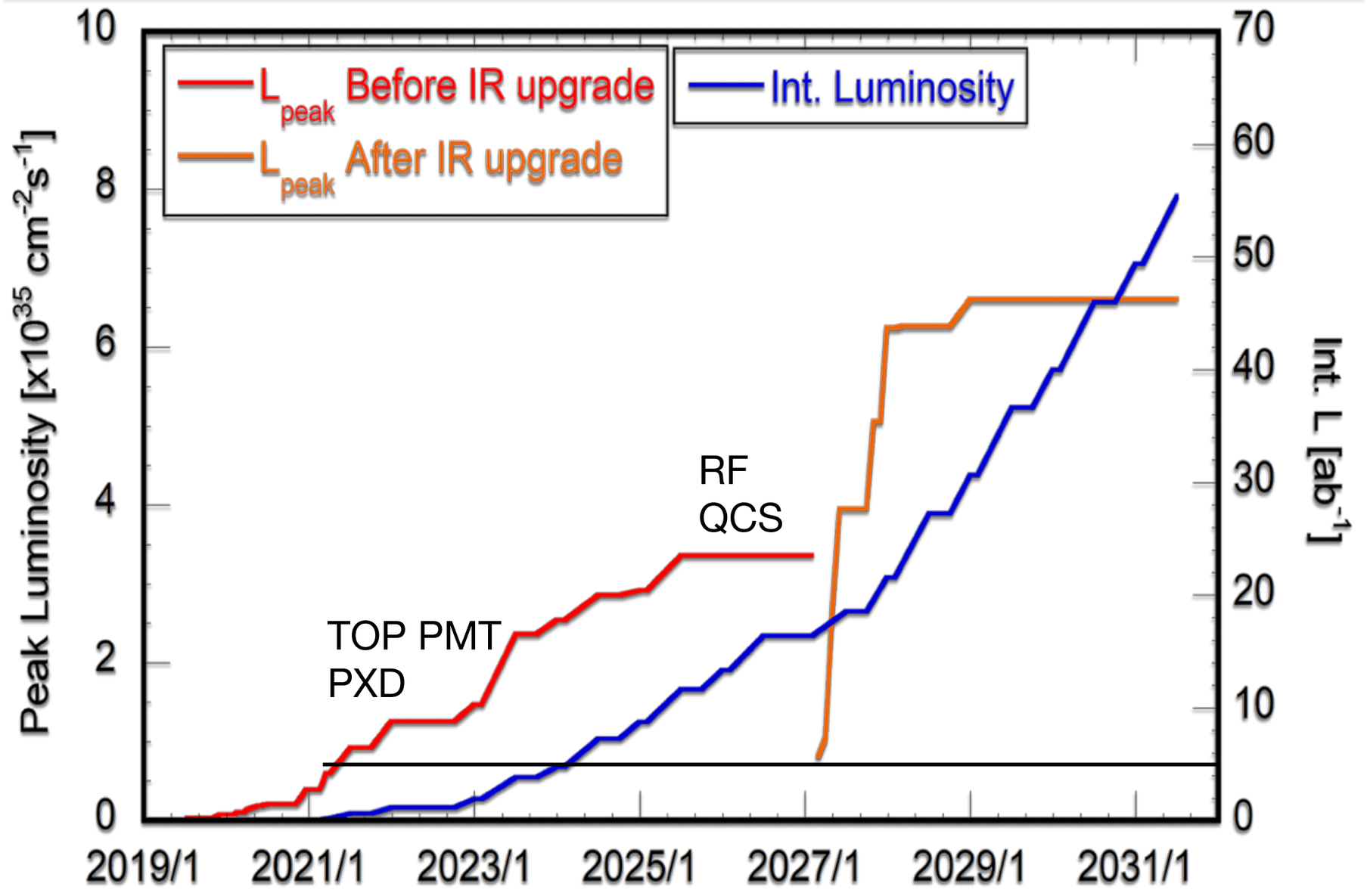
Central Drift Chamber (CDC)
- He (50%), C_2H_6 (50%), small cells, fast electrics

Particle ID detector
- Barrel: Time-Of-Propagation counters (TOP)
- Endcap: Aerogel RICH (ARICH)

ElectroMagnetic Calorimeter (ECL)
- CsI(Tl) + waveform sampling

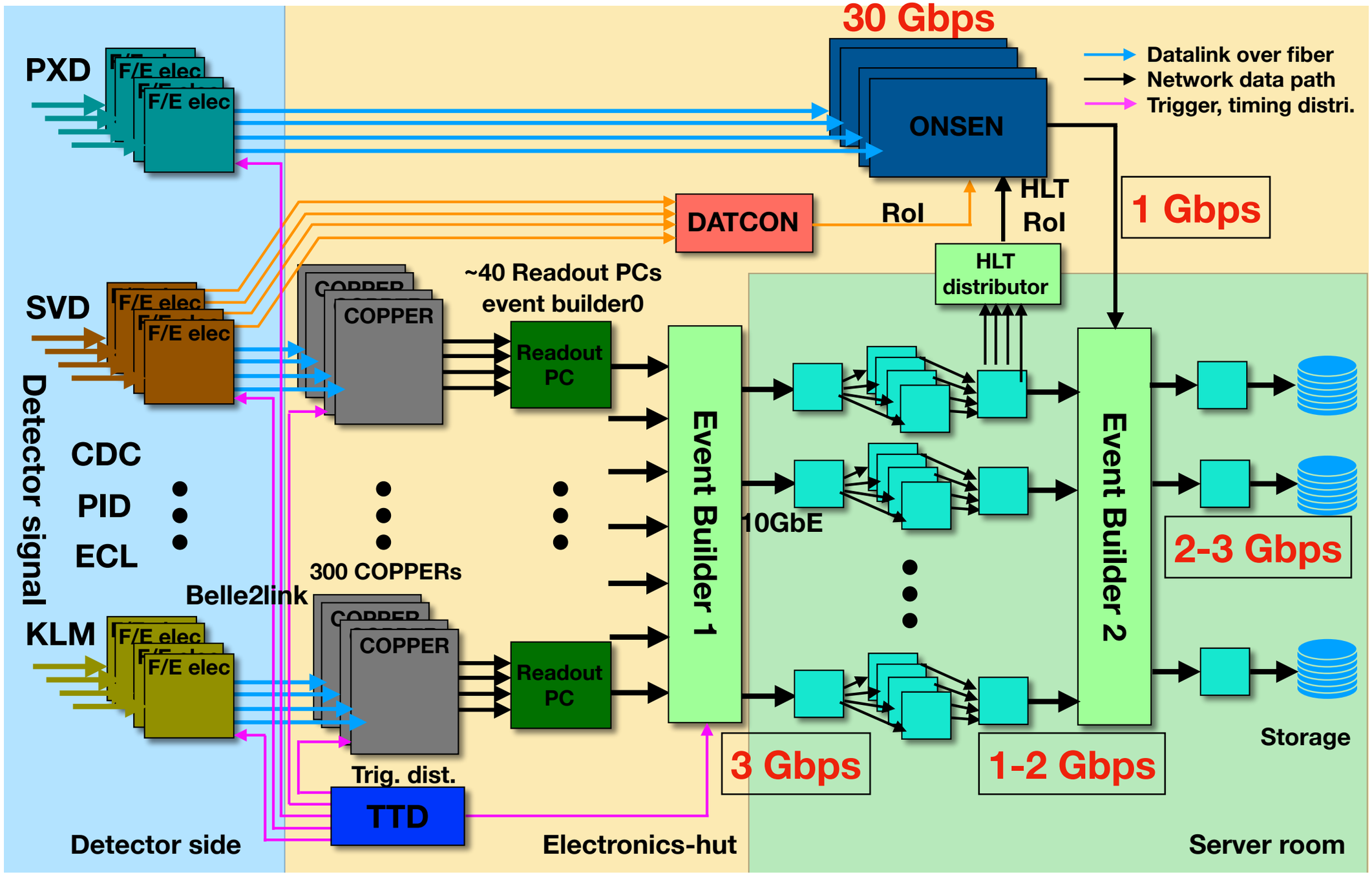
K_L/μ detector (KLM)
- Outer barrel: Resistive Plate Counter (RPC)
- Endcap/inner barrel: Sci.

Luminosity prospects



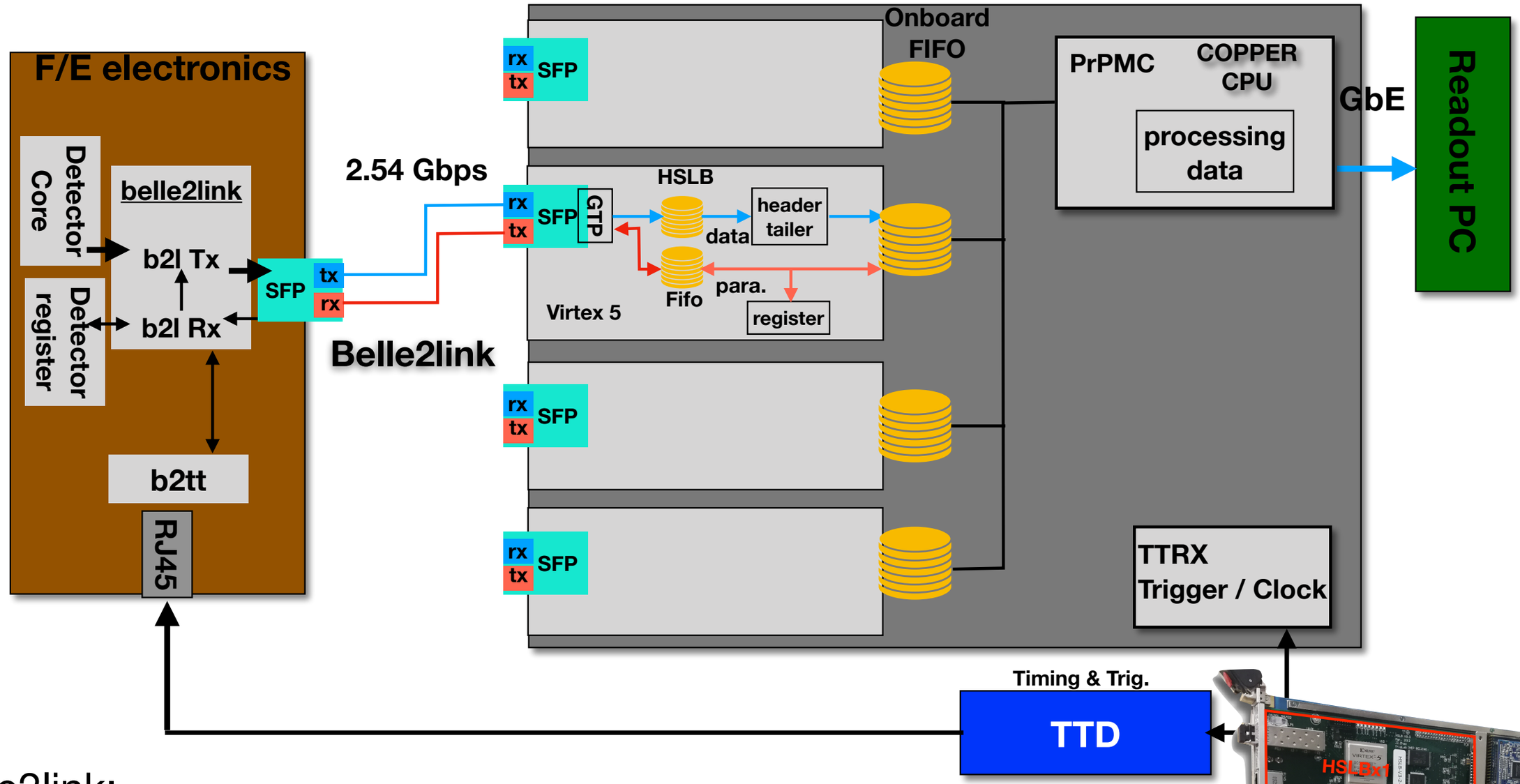
- Integrated luminosity is expected to reach 1 ab^{-1} by the end of 2021, comparable with Belle/Babar
- Accumulate 50 ab^{-1} by 2031
- Planed long showdown
  - 2022: MCP-PMT of TOP replacement, PXD replacement
  - 2026: Improvement of RF, QCS modification

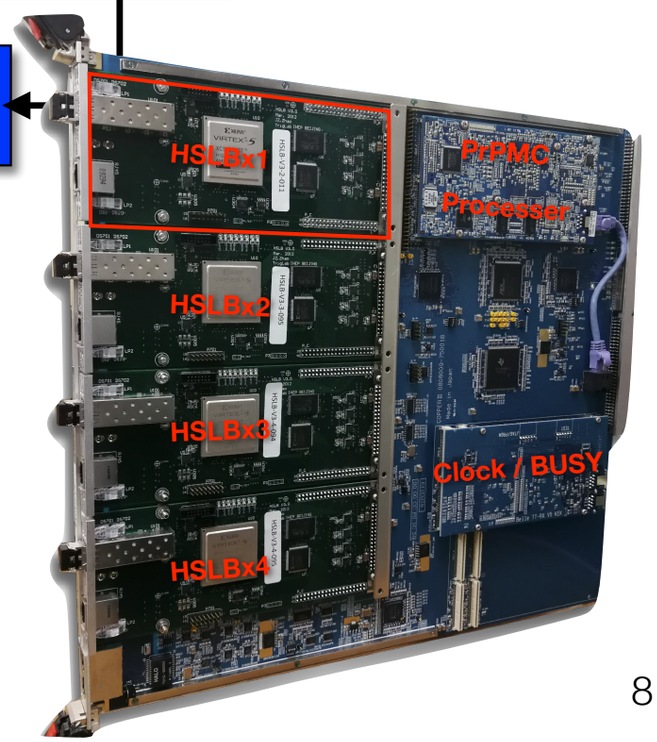
Belle II DAQ system



- Unified common readout system for sub-detectors (except for PXD)
- Unified timing and trigger distribution system
- A pipeline readout
- To handle 30 kHz level 1 trigger with ∅ 1% dead time under raw event size of 1 MB

Readout system





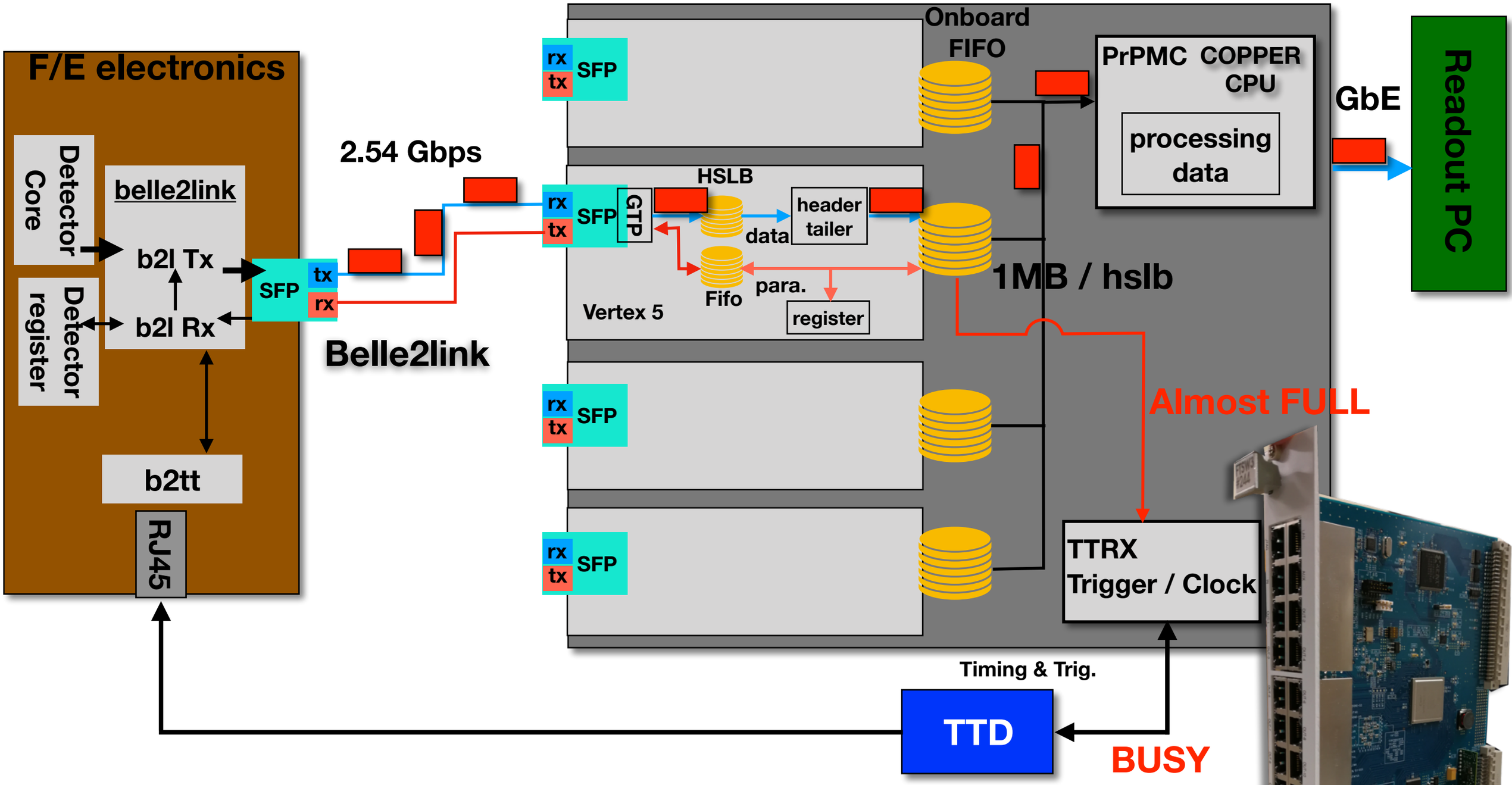
Belle2link:

Unified high speed optical link (2.54Gbps) connected Front-End Electronics and DAQ readout board (COPPER-HSLB), data transmission based on Rocket I/O.

Functionalities of readout system

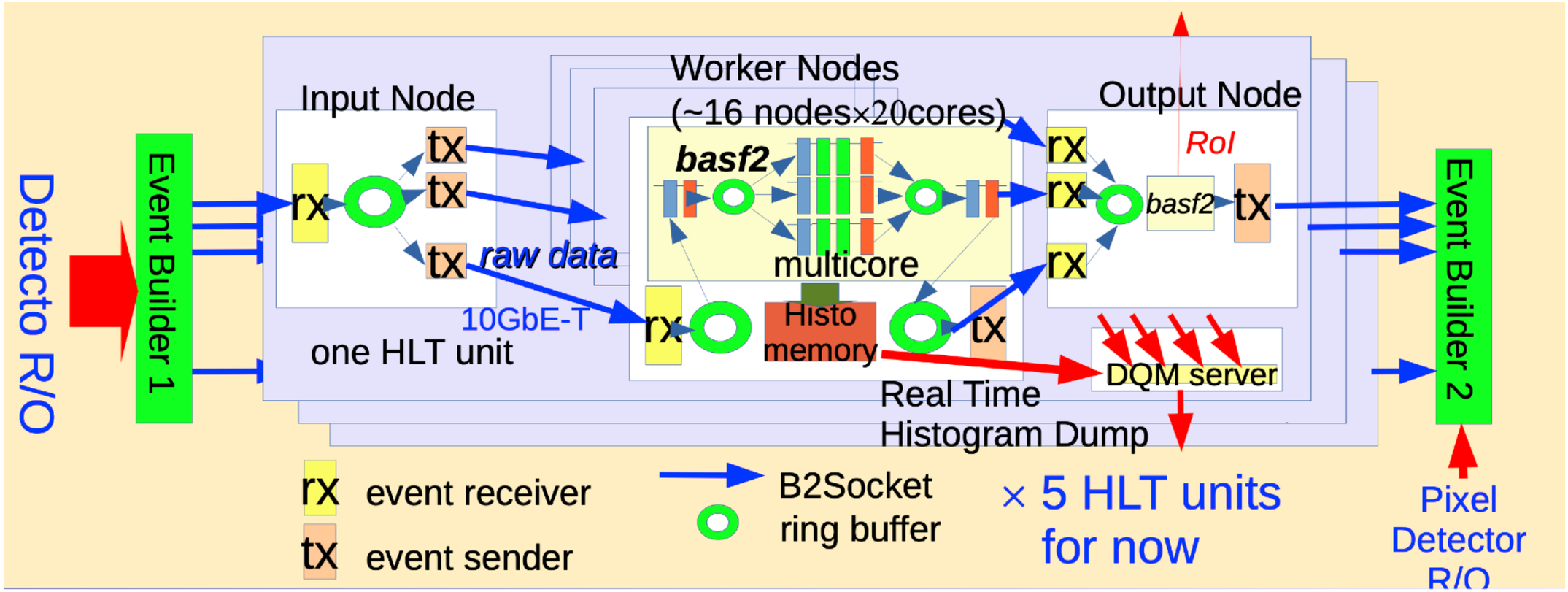
- Belle2link,
- TTD interface,
- slow control,
- pre event-building, GbE
- Data-formatting
- Data-check

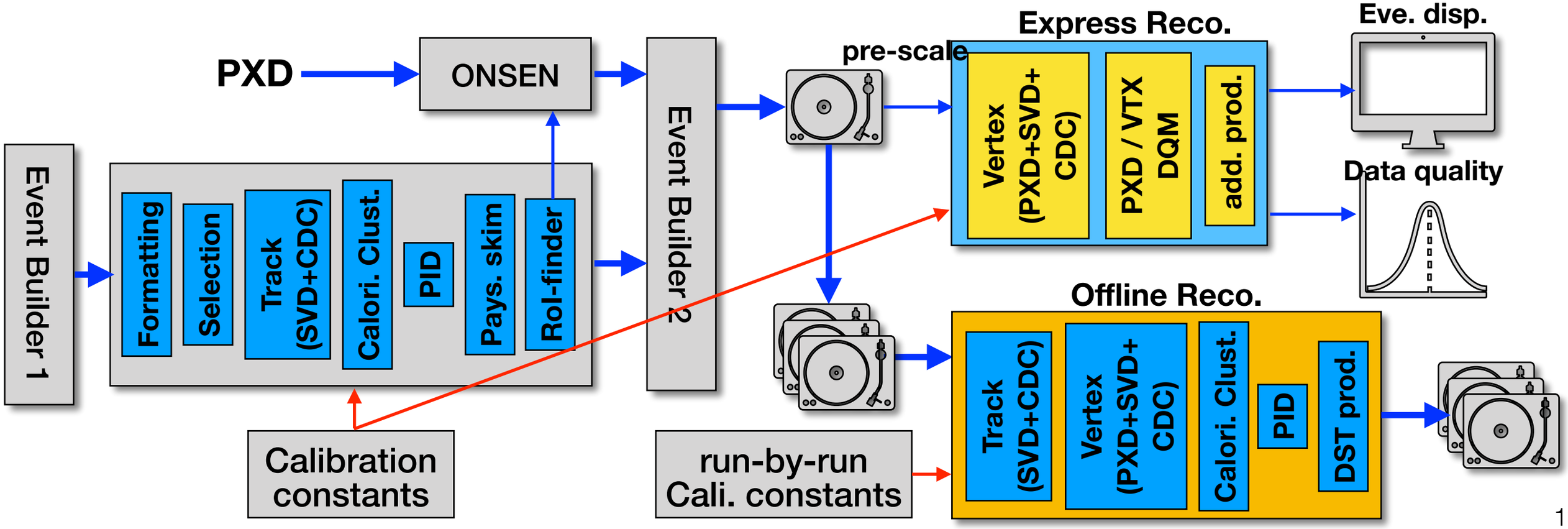
Trigger and busy handshake



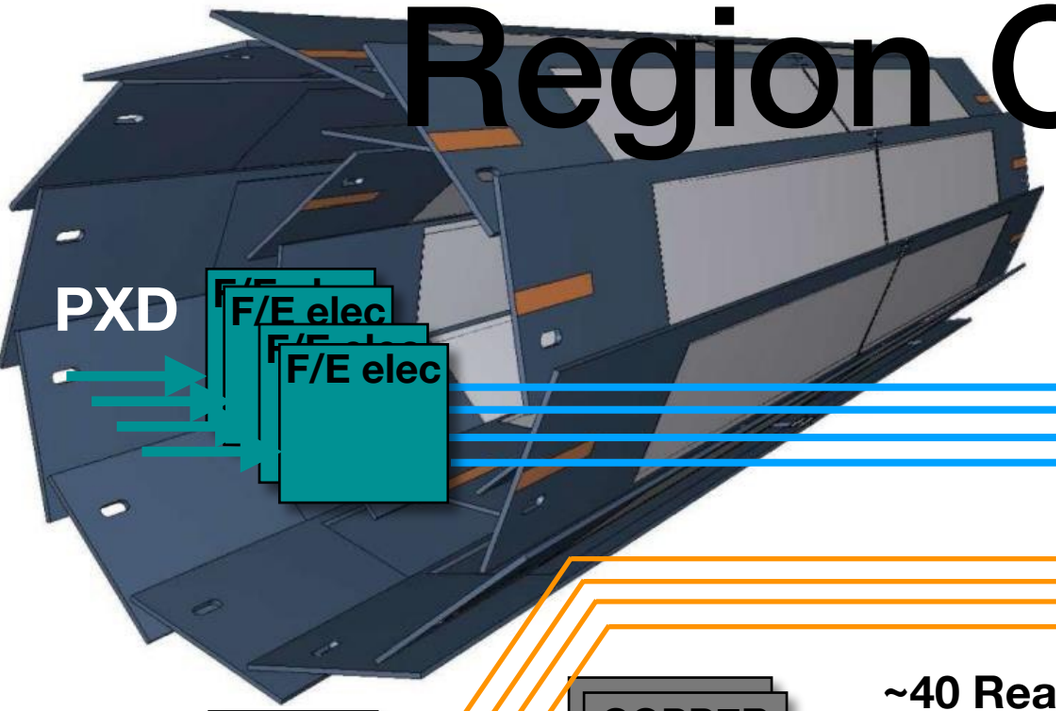
- To avoid buffer overflow, BUSY signal used to stop issue trigger
- BUSY signal connected to Timing and Trigger Distribution (TTD) system
- FTSW module: serial link protocol driven by Vritex 5 FPGA
  - 20 RJ-45 ports, used for b2tt or JTAG
  - Tree structure with one master and slaves FTSW module

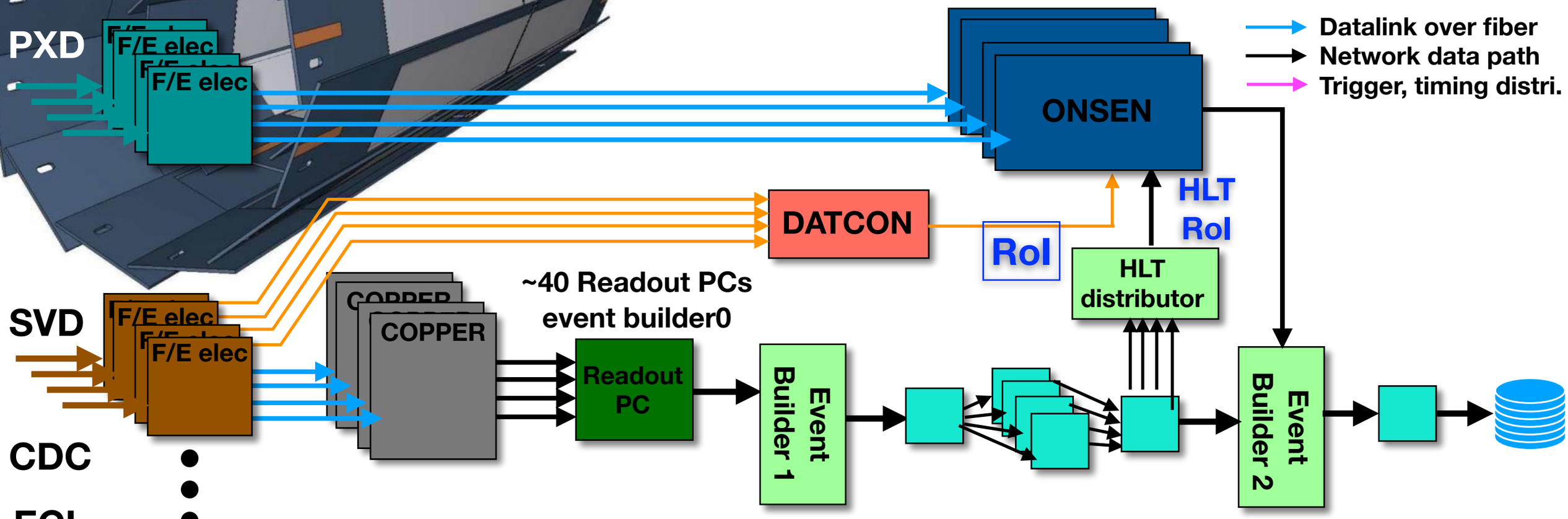
High Level Trigger (HLT)



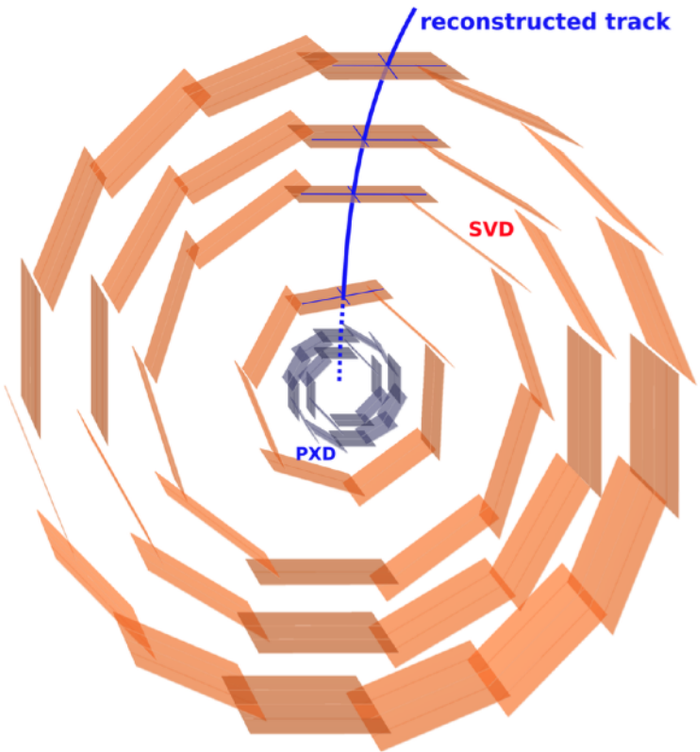


Region Of Interest (ROI)

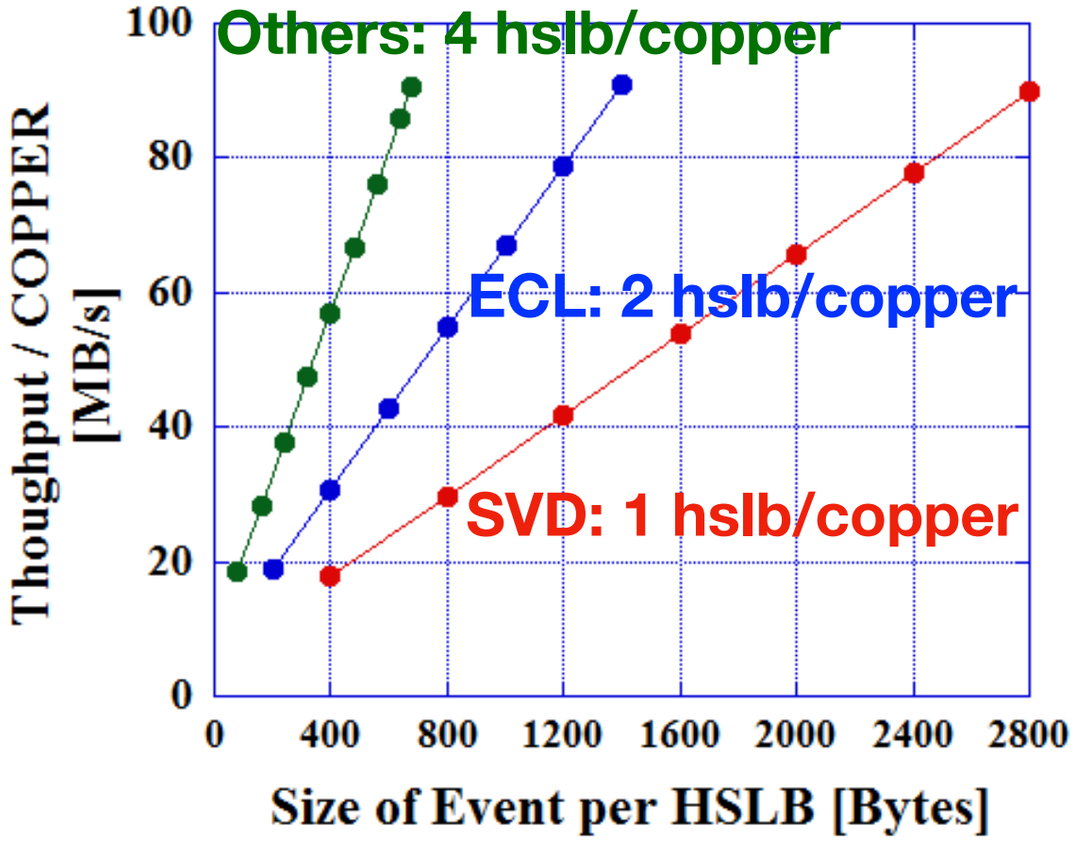




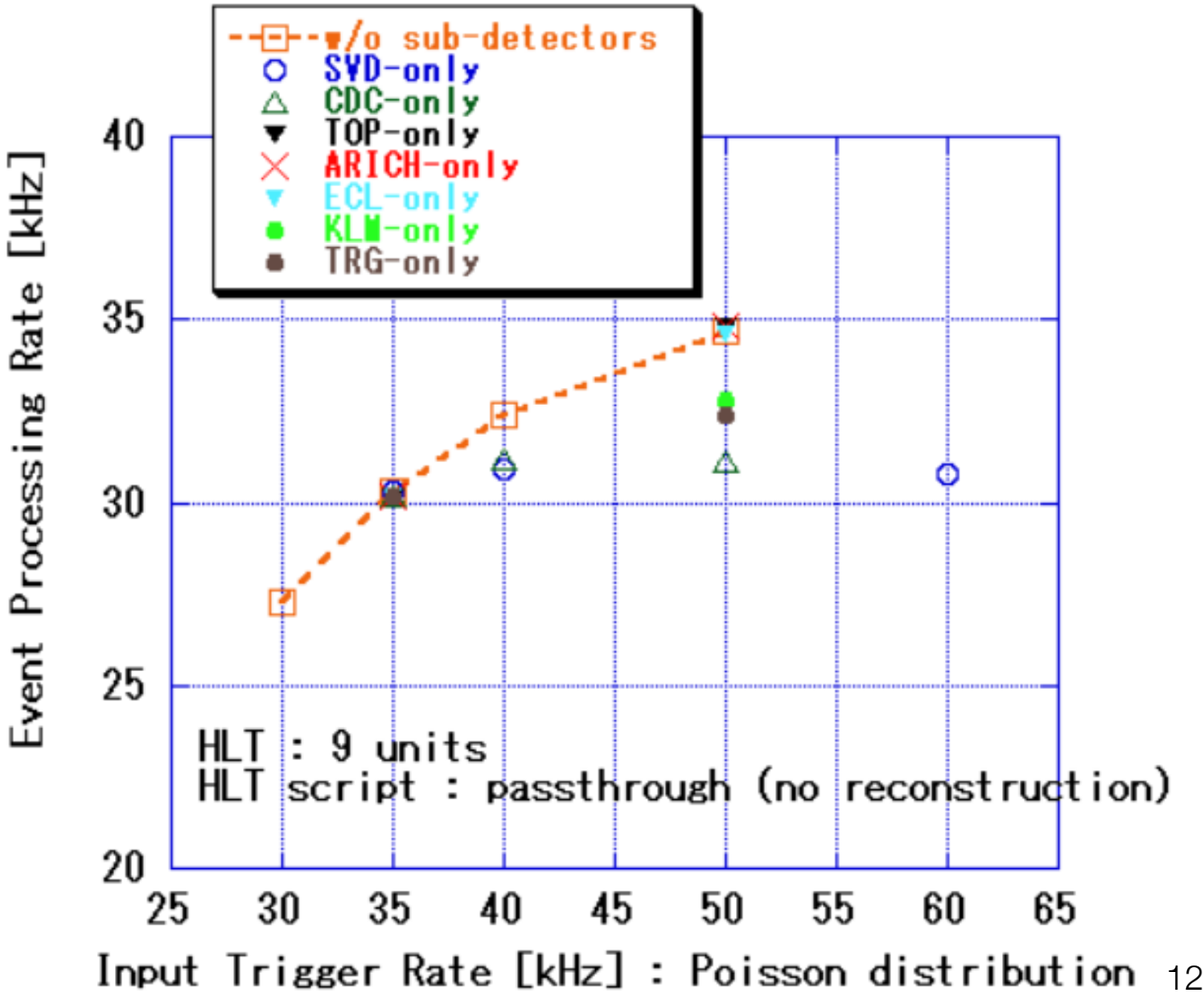
- PXD event size = 1MB/event, 10 times larger than the rest of detectors
- Region of interest method is effective to reduce the data size
- ROI
  - Tracking software running on HLT nodes
  - Fast method: SVD tracks finding base on FPGA by dedicated AMC module (DATCON)
- PXD event data size reduced by 1/10 with ROI
  - In addition, trigger rate reduced by 1/3 with HLT ROI



Stress test for DAQ readout system

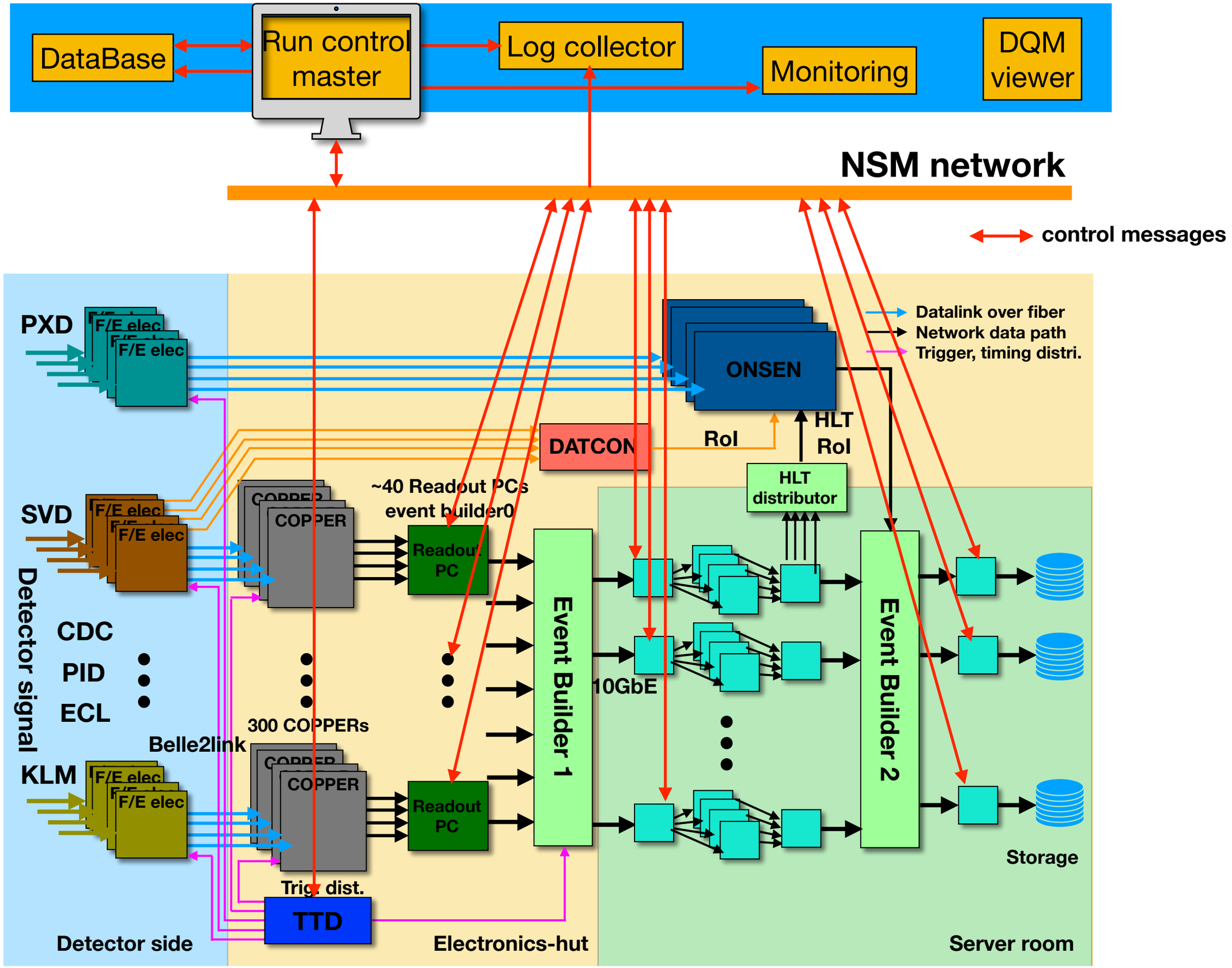


- Operation with 30 kHz input trigger rate was achieved
- Throughout of belle2link and Gigabit Ethernet to readout PC is enough to handle 30 kHz operation



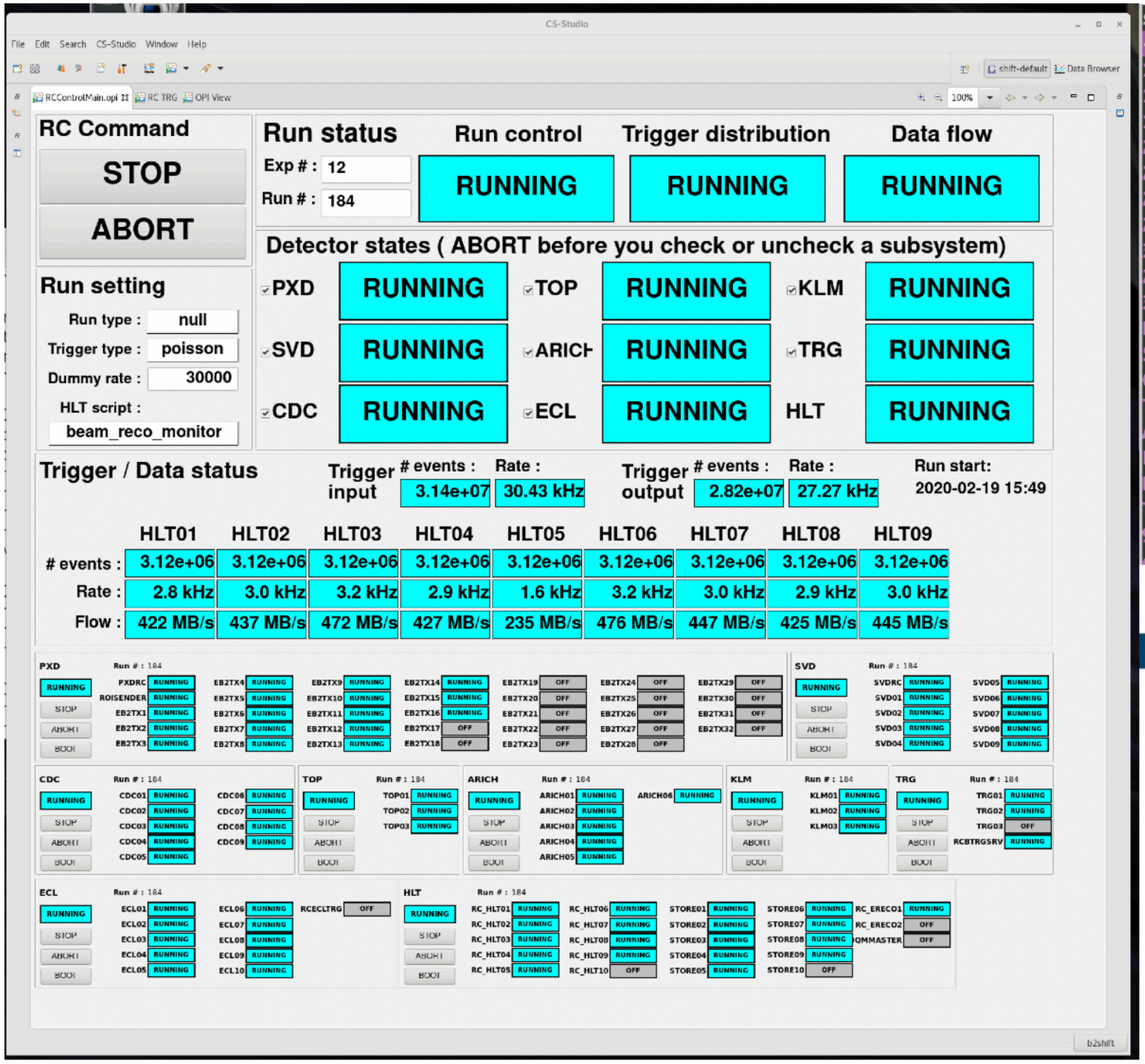
- Above 30 kHz trigger input, the processing rate is suppressed to avoid SVD FEE's buffer overflow
- Some sub-detectors observed a limit due to the throughout bandwidth (2Gbps) between COPPER to readout PC

Belle II slow control system

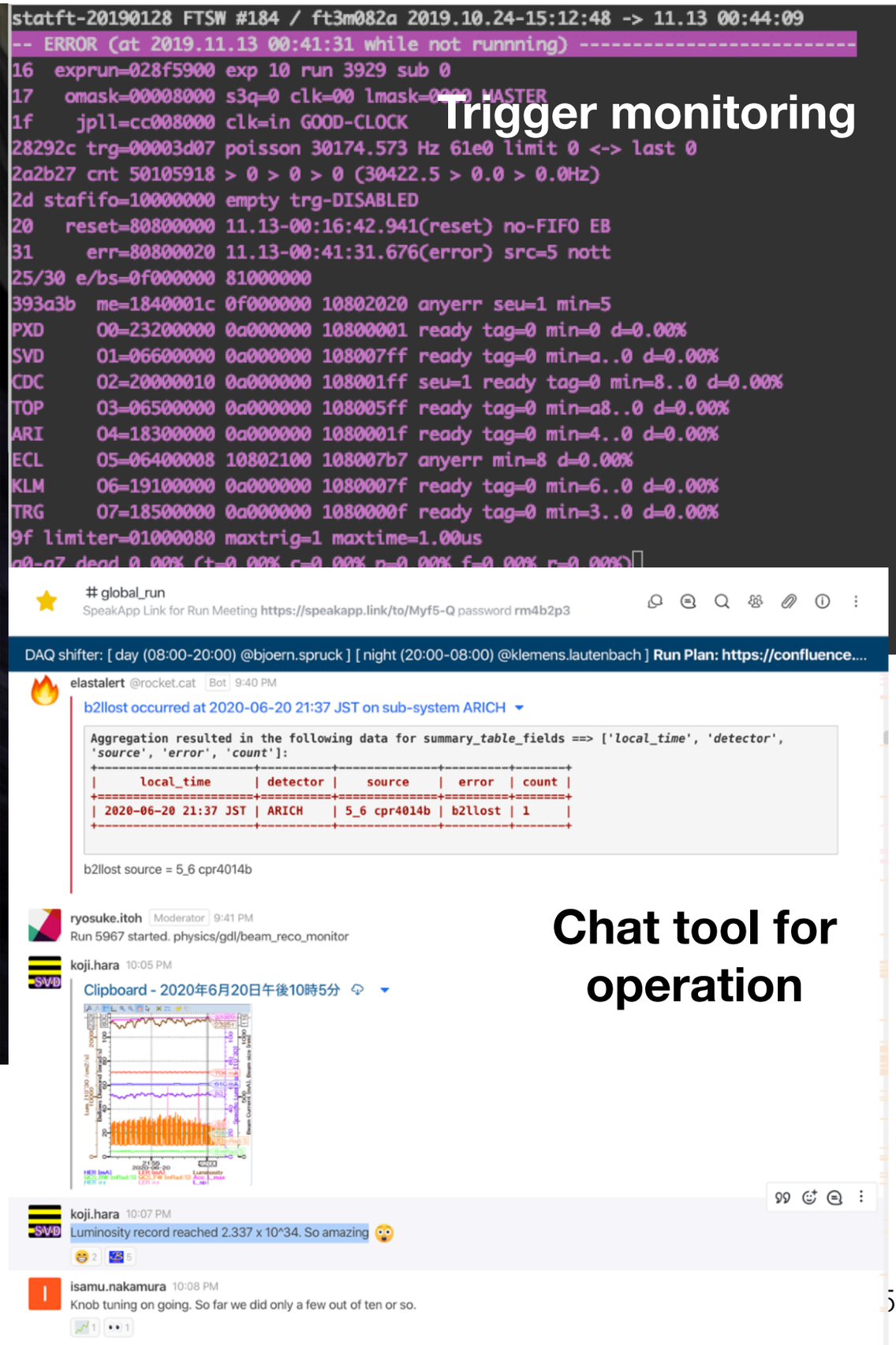


Control room

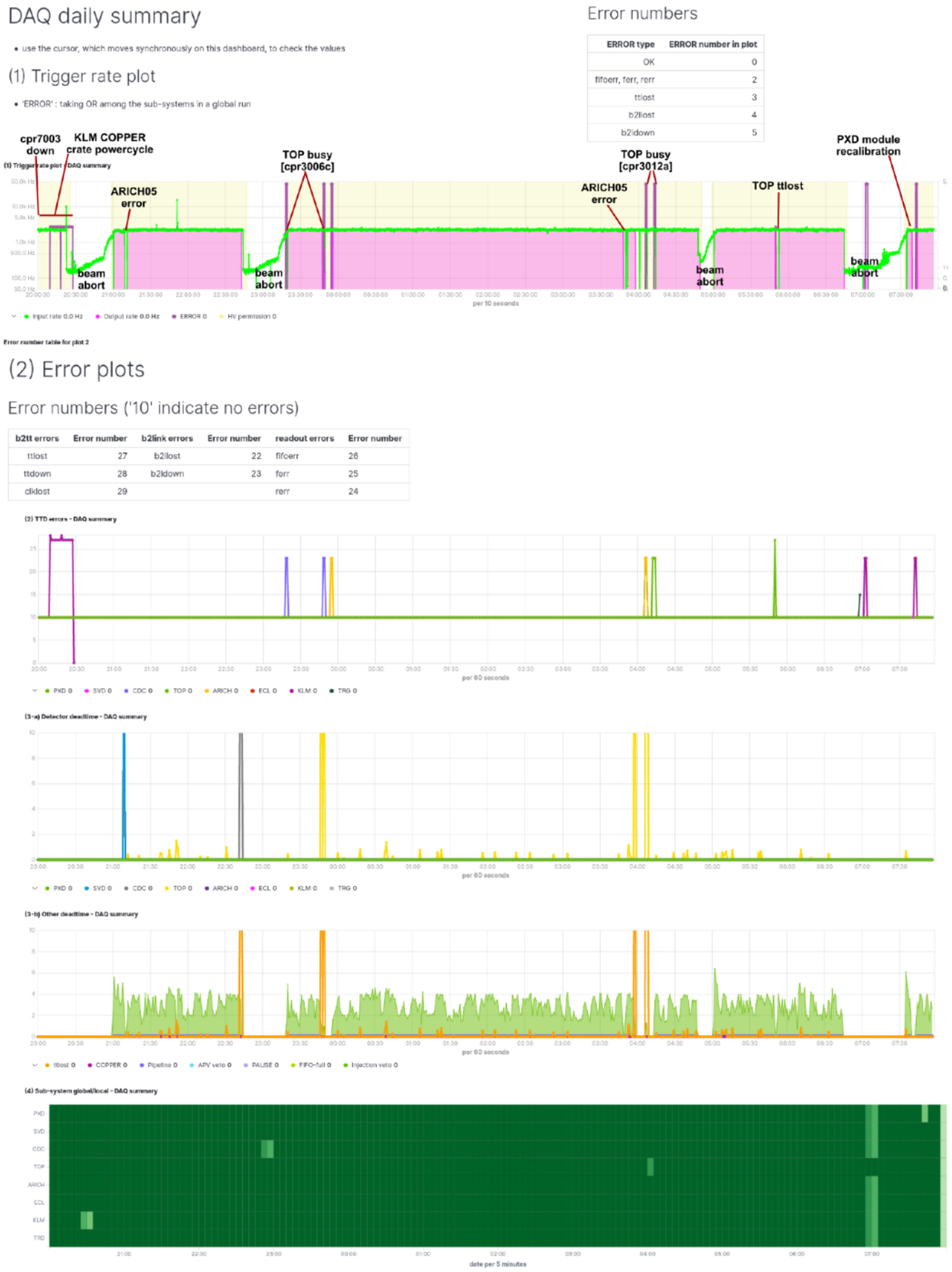
Run control



GUI run control panel

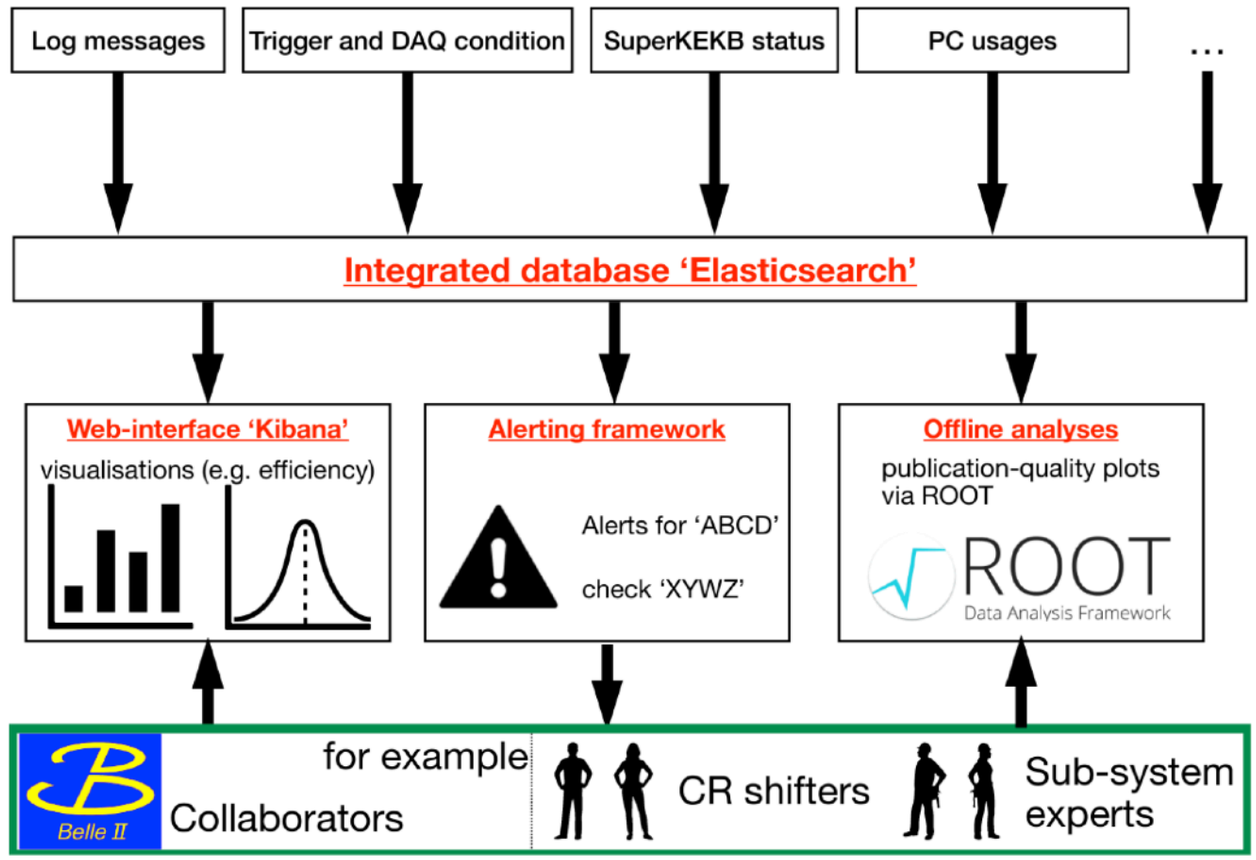


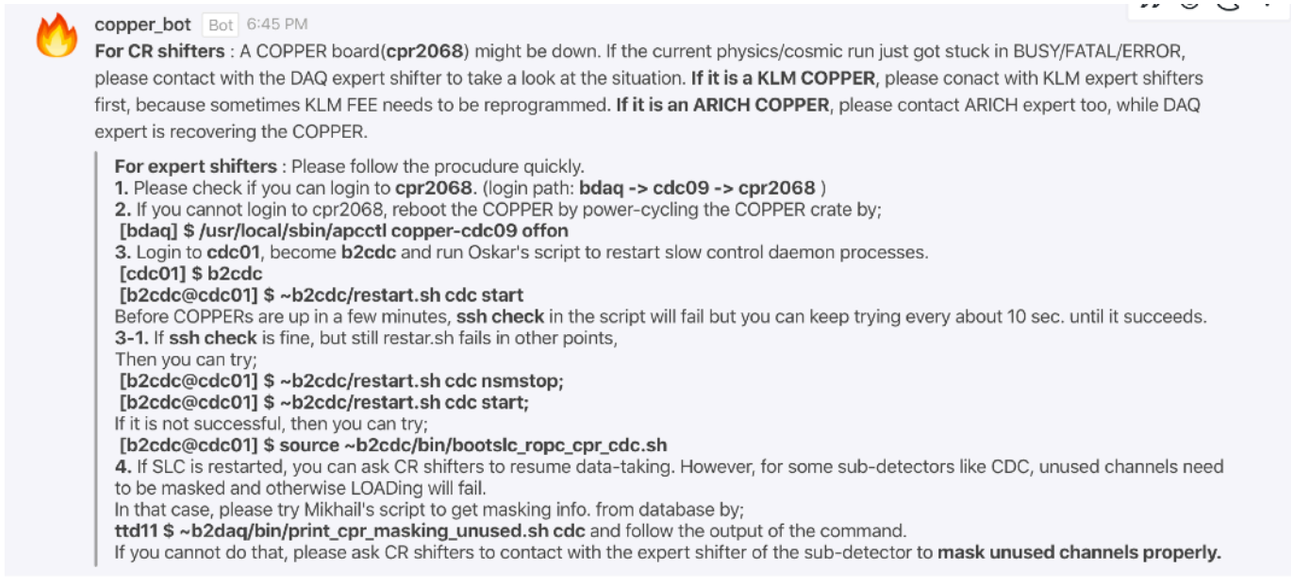
Monitoring system (ELK)



Error numbers

ERROR type	ERROR number in plot
OK	0
fifoerr, ferr, rerr	2
ttlost	3
b2llost	4
b2ldown	5



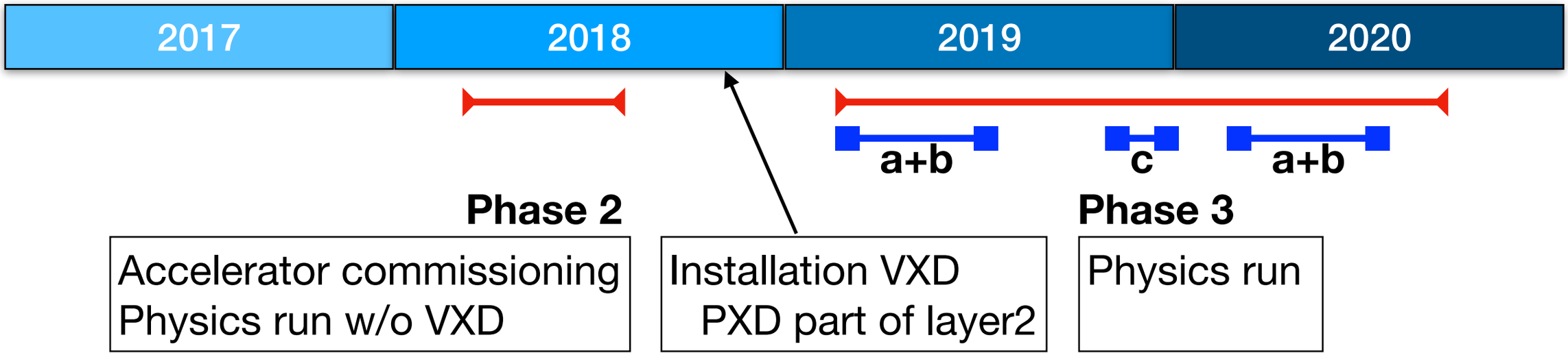


copper_bot Bot 6:45 PM

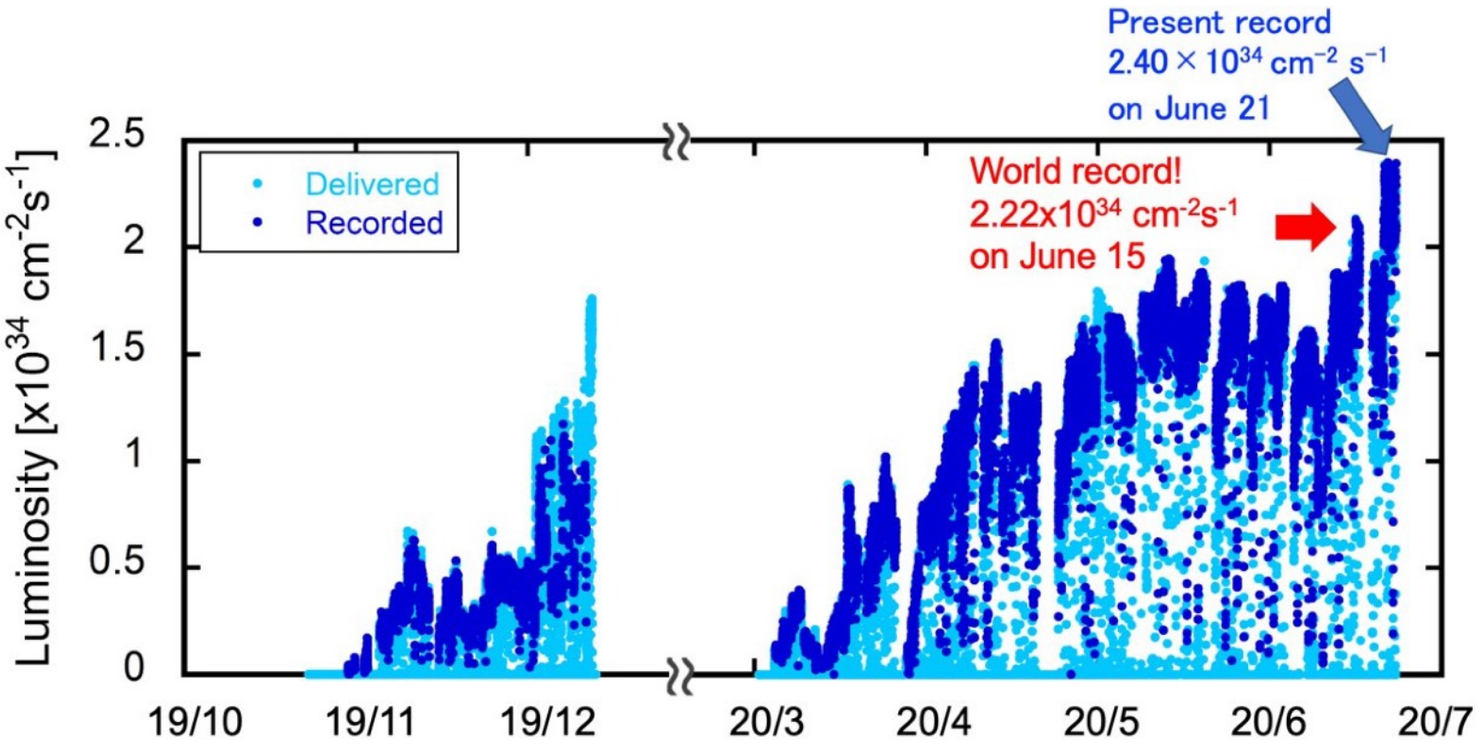
For CR shifters : A COPPER board(**cpr2068**) might be down. If the current physics/cosmic run just got stuck in BUSY/FATAL/ERROR, please contact with the DAQ expert shifter to take a look at the situation. **If it is a KLM COPPER**, please conact with KLM expert shifters first, because sometimes KLM FEE needs to be reprogrammed. **If it is an ARICH COPPER**, please contact ARICH expert too, while DAQ expert is recovering the COPPER.

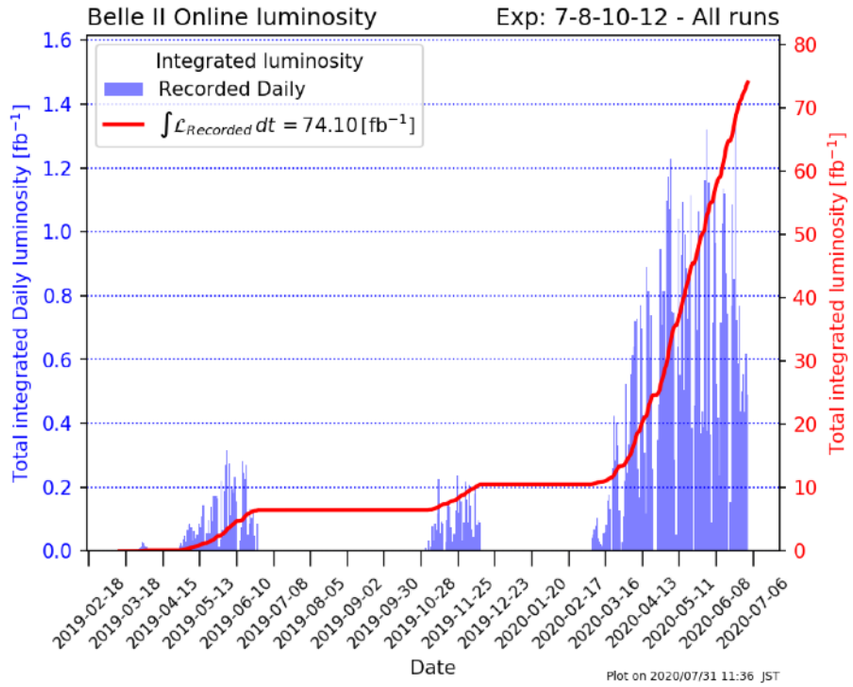
> **For expert shifters** : Please follow the procudure quickly.
> **1.** Please check if you can login to **cpr2068**. (login path: **bdaq -> cdc09 -> cpr2068**)
> **2.** If you cannot login to cpr2068, reboot the COPPER by power-cycling the COPPER crate by;
> **[bdaq] $ /usr/local/sbin/apcctl copper-cdc09 offon**
> **3.** Login to **cdc01**, become **b2cdc** and run Oskar's script to restart slow control daemon processes.
> **[cdc01] $ b2cdc**
> **[b2cdc@cdc01] $ ~b2cdc/restart.sh cdc start**
> Before COPPERs are up in a few minutes, **ssh check** in the script will fail but you can keep trying every about 10 sec. until it succeeds.
> **3-1.** If **ssh check** is fine, but still restar.sh fails in other points,
> Then you can try;
> **[b2cdc@cdc01] $ ~b2cdc/restart.sh cdc nsmstop;**
> **[b2cdc@cdc01] $ ~b2cdc/restart.sh cdc start;**
> If it is not successful, then you can try;
> **[b2cdc@cdc01] $ source ~b2cdc/bin/bootslc_ropc_cpr_cdc.sh**
> **4.** If SLC is restarted, you can ask CR shifters to resume data-taking. However, for some sub-detectors like CDC, unused channels need to be masked and otherwise LOADing will fail.
> In that case, please try Mikhail's script to get masking info. from database by;
> **ttd11 $ ~b2daq/bin/print_cpr_masking_unused.sh cdc** and follow the output of the command.
> If you cannot do that, please ask CR shifters to contact with the expert shifter of the sub-detector to **mask unused channels properly.**

SuperKEKB/BelleII run status



- **Belle II under COVID-19**
  - **1 local CR shifter + 1 remote shifter**
  - **1 BCG shifter (local only)**
  - **Expert shifters (remotely)**

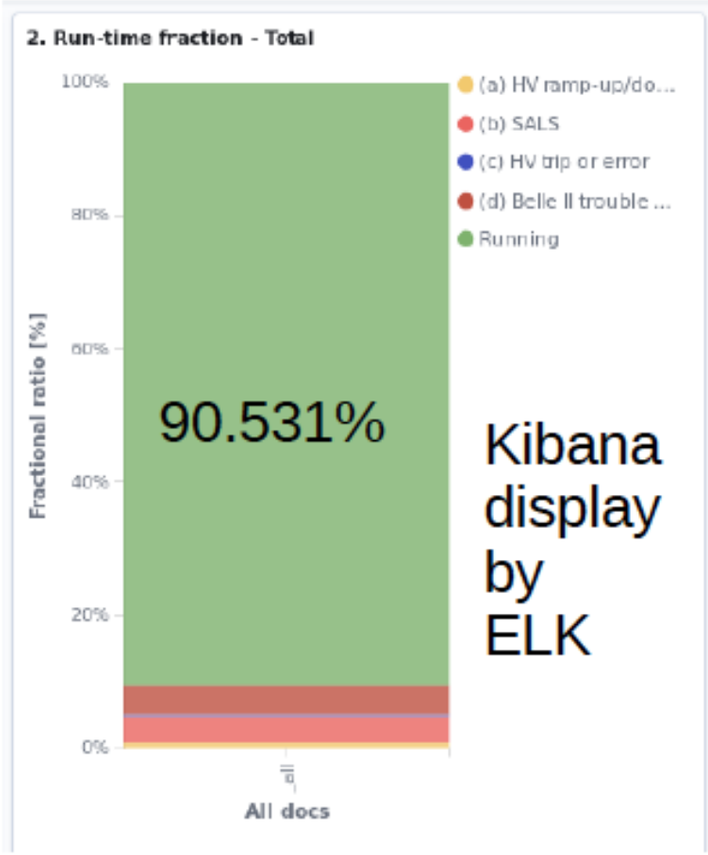




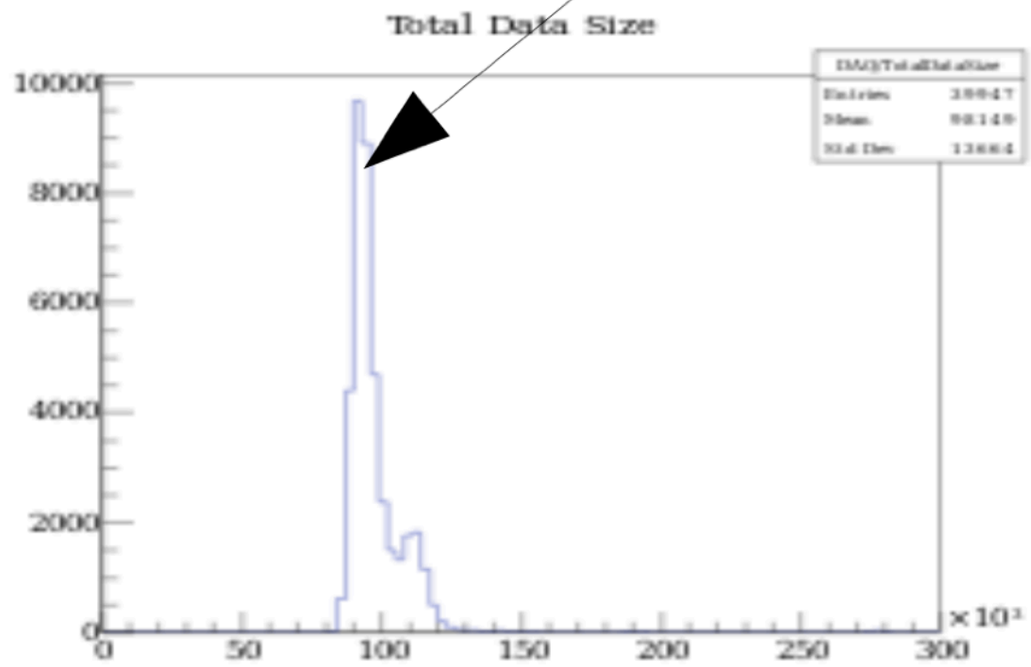
DAQ performance in 2020ab

- DAQ efficiency is about 90% (include injection veto)
  - Level 1 trigger rate up to 5 kHz
- 9 HLT units (3000 cores) are operated with newly implemented with Zero-MQ HLT, improved the stability
- Newly implemented monitoring system (ELK) is extensively used to monitor the system and report issues

- Typical DAQ troubles
  - COPPER CPU freeze
  - link error
    - COPPER-HSLB <—> FEEs
    - FTSW <—> FEEs
  - Data corruption

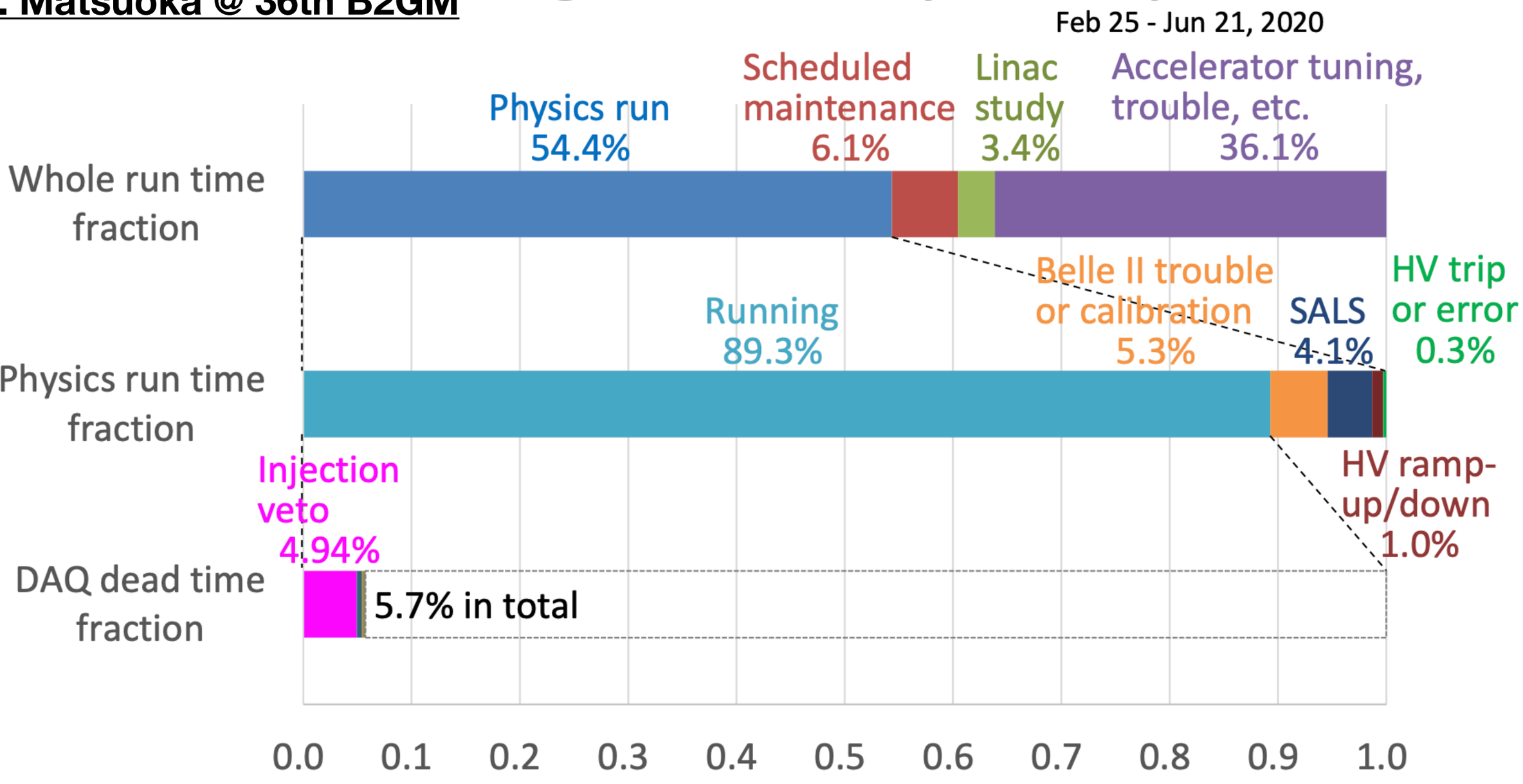


Express Reco. ~ 100 kB / event



Data taking efficiency in 2020ab

K. Matsuoka @ 36th B2GM



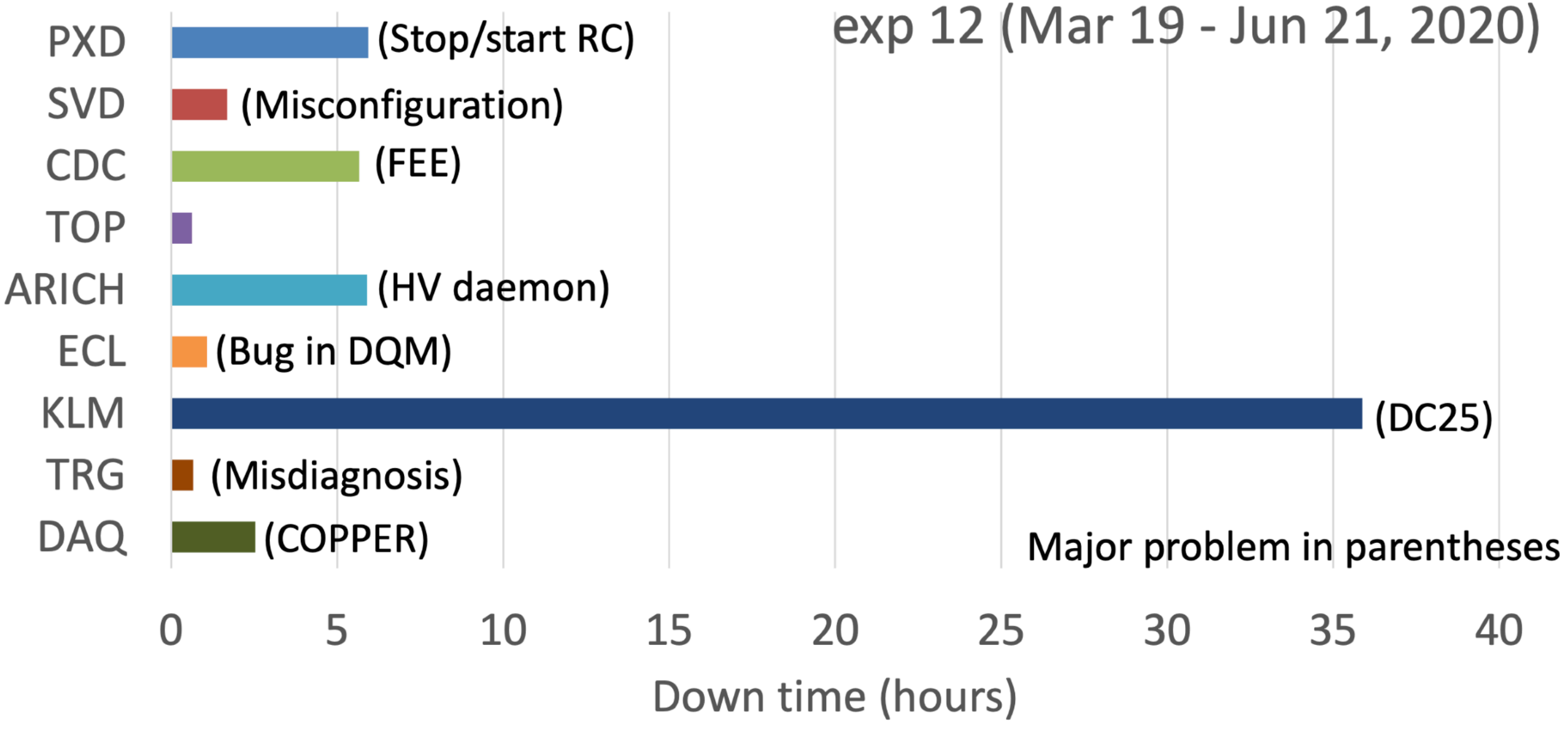
Overall data taking efficiency

84.2% (Target 90%)

cf. 47.0% (exp 7), 64.9% (exp 8), 49.1-55.2% (exp 10)

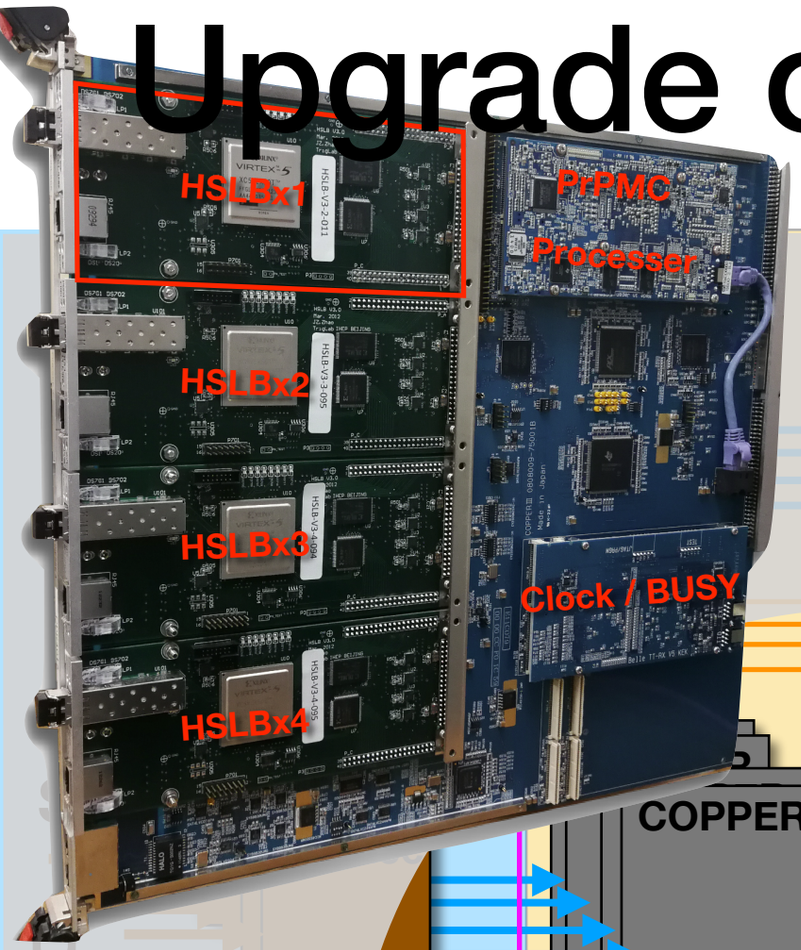
Major downtime in 2020ab

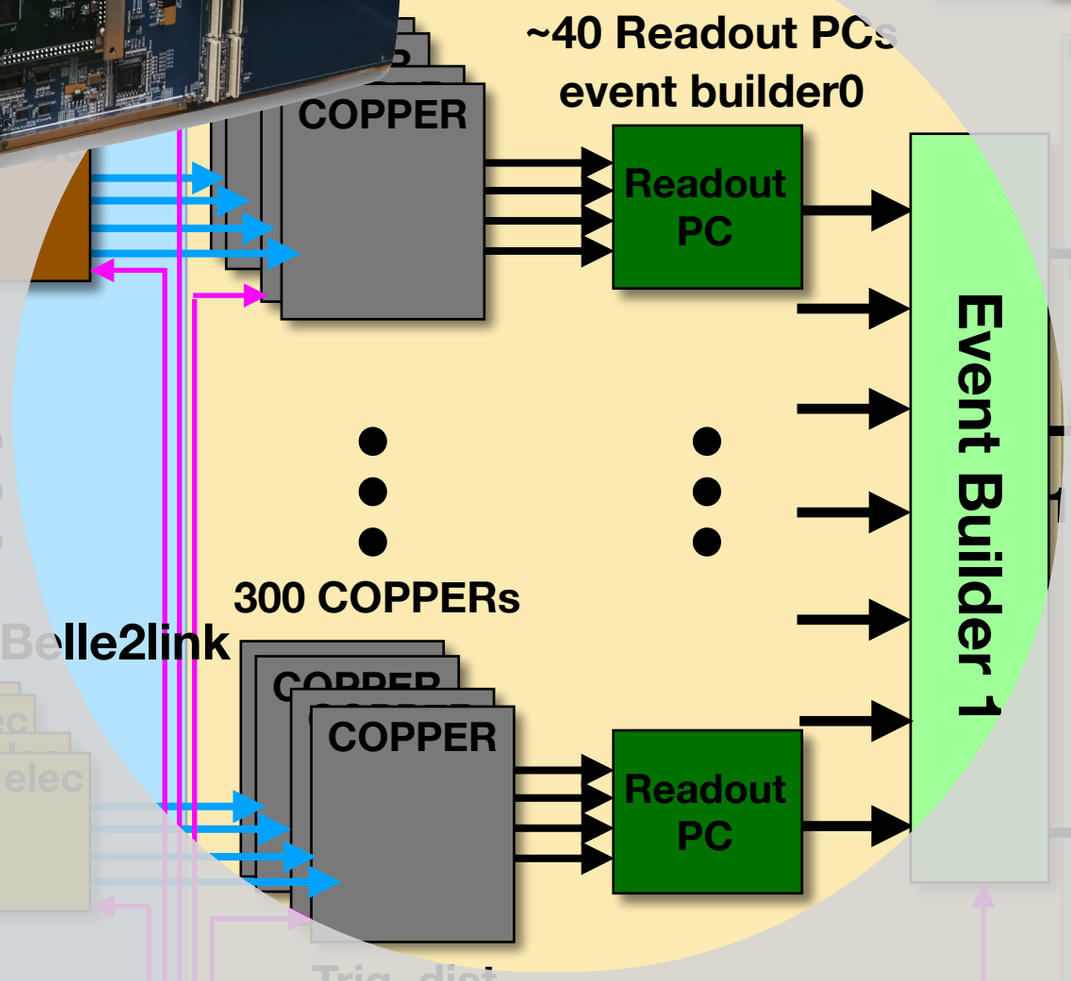
K. Matsuoka @ 36th B2GM



Belle II DAQ upgrade

Upgrade of Belle II readout system

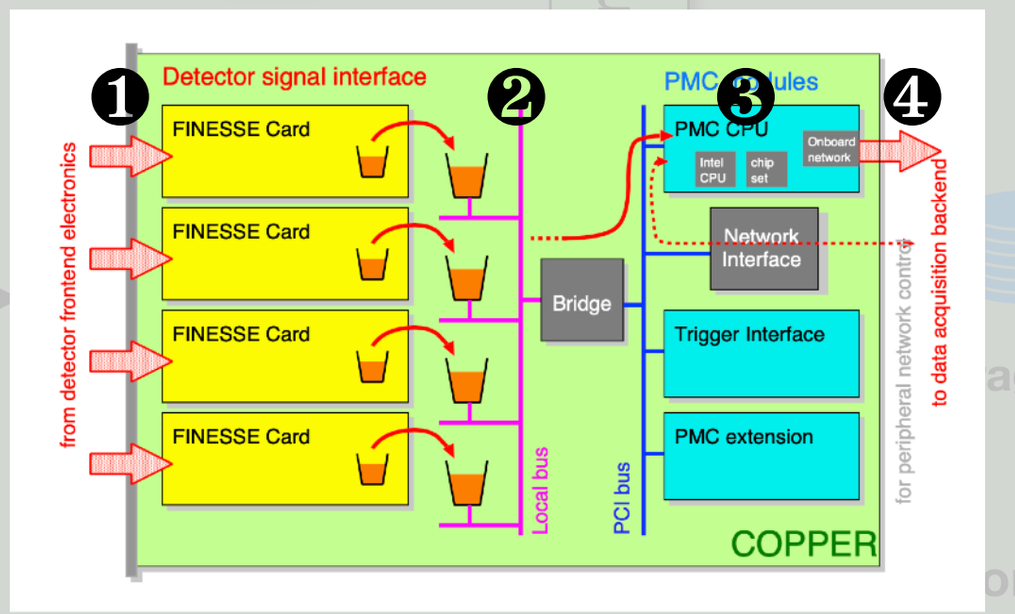




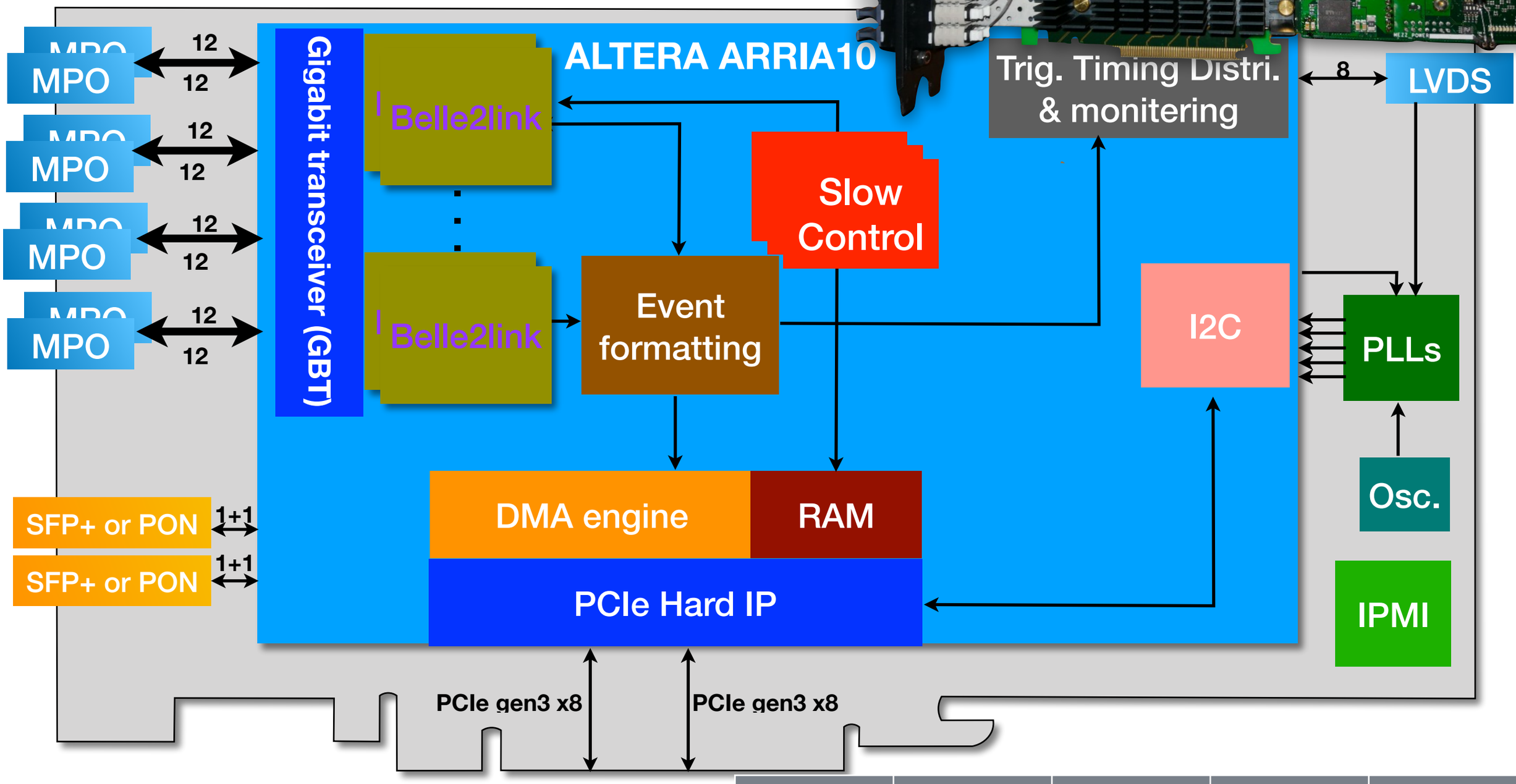
❶ ❷ ❹

2.54 Gbps > 130 MBps ~ 125 MBps

- **Difficult to maintain during the entire Belle II operation period (10 years)**
  - **Four different boards**
  - **Discontinued parts are increasing (chipset on PrPMC card …)**
- **Limitation to improve DAQ performance**
  - **Bottlenecks of COPPER**
    - **CPU usage**
    - **Data transfer speed (1 Gbps)**
- **Bottleneck of network output of ROPC (1 Gbps)**
- **Luminosity & background situation changed**



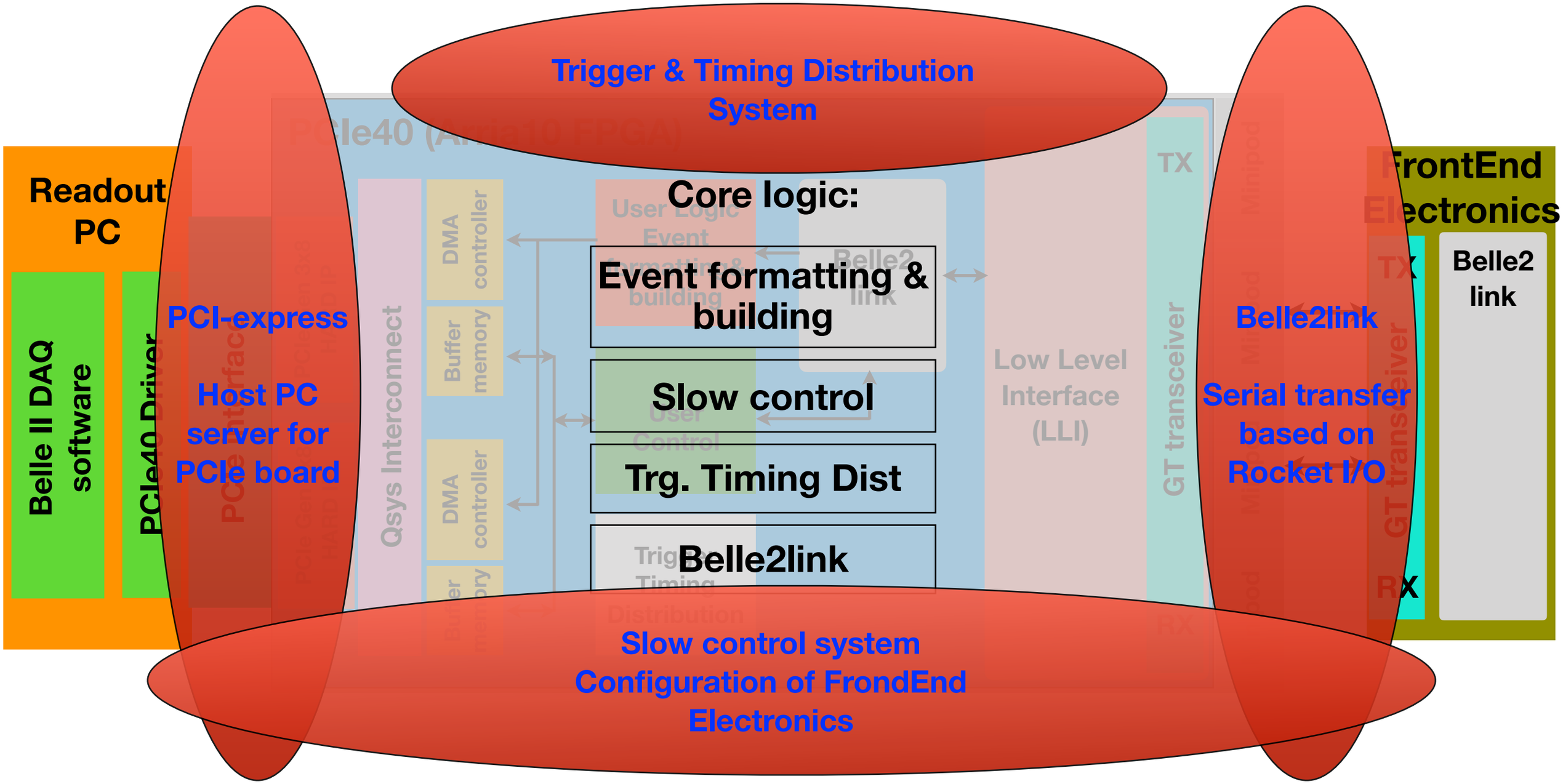
PCIe40 module



19 PCIe40 boards to replace ~300 COPPERs

Board	FPGA family	Optical links	PC interface	Experiment
PCIe40 (IJClab)	ALTERA Arria10	24x2	2 PCIe Gen3 x 8	LHCb, ALICE

New readout system

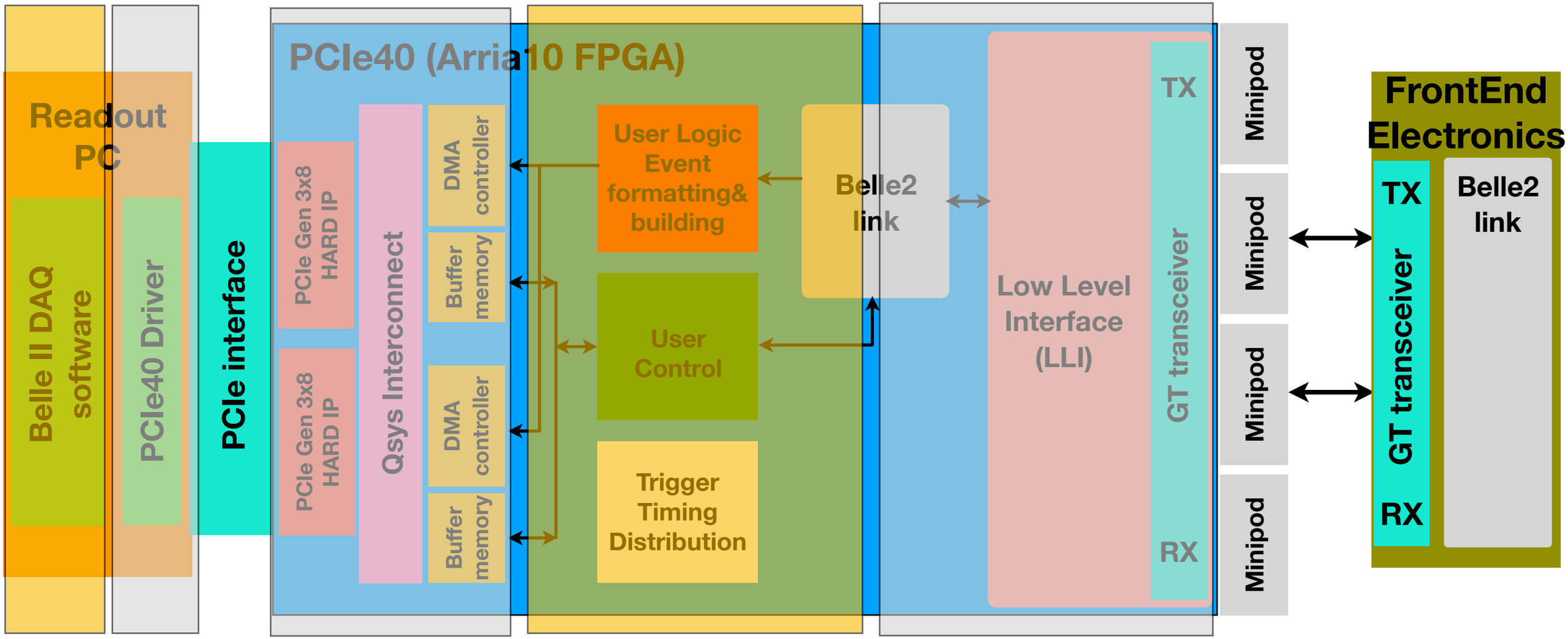


- **Upgrade of readout system will keep the modification as small as possible, for the system connected. No major modification required for the other systems.**

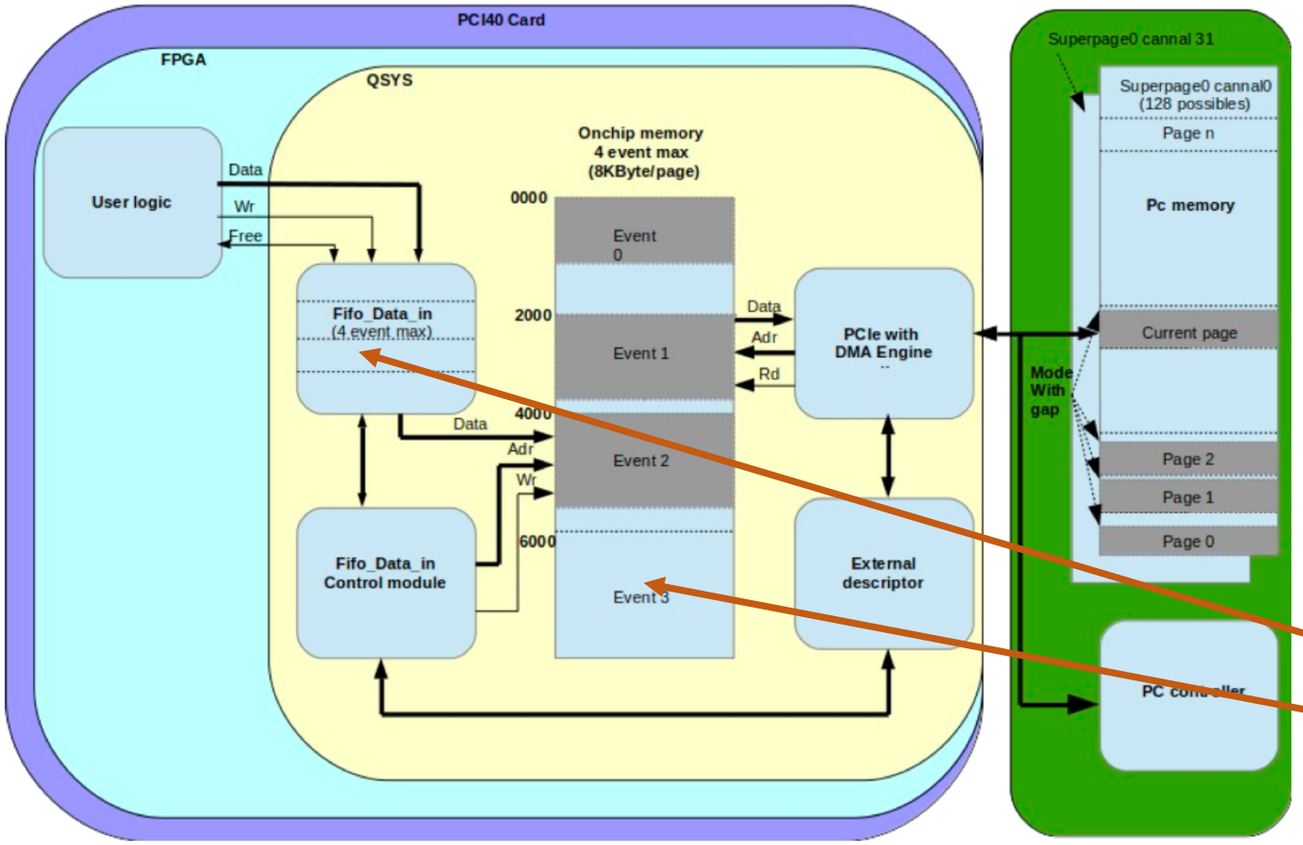
Development of firmware and software

Pcie40 (low-level) firmware and software driver: IJClab + Krakow experts

TTD interface, userlogic, slow control, DAQ software: others Belle II DAQ members
KEK, Nagoya, Hawaii, Louisville, etc.



DMA implementation

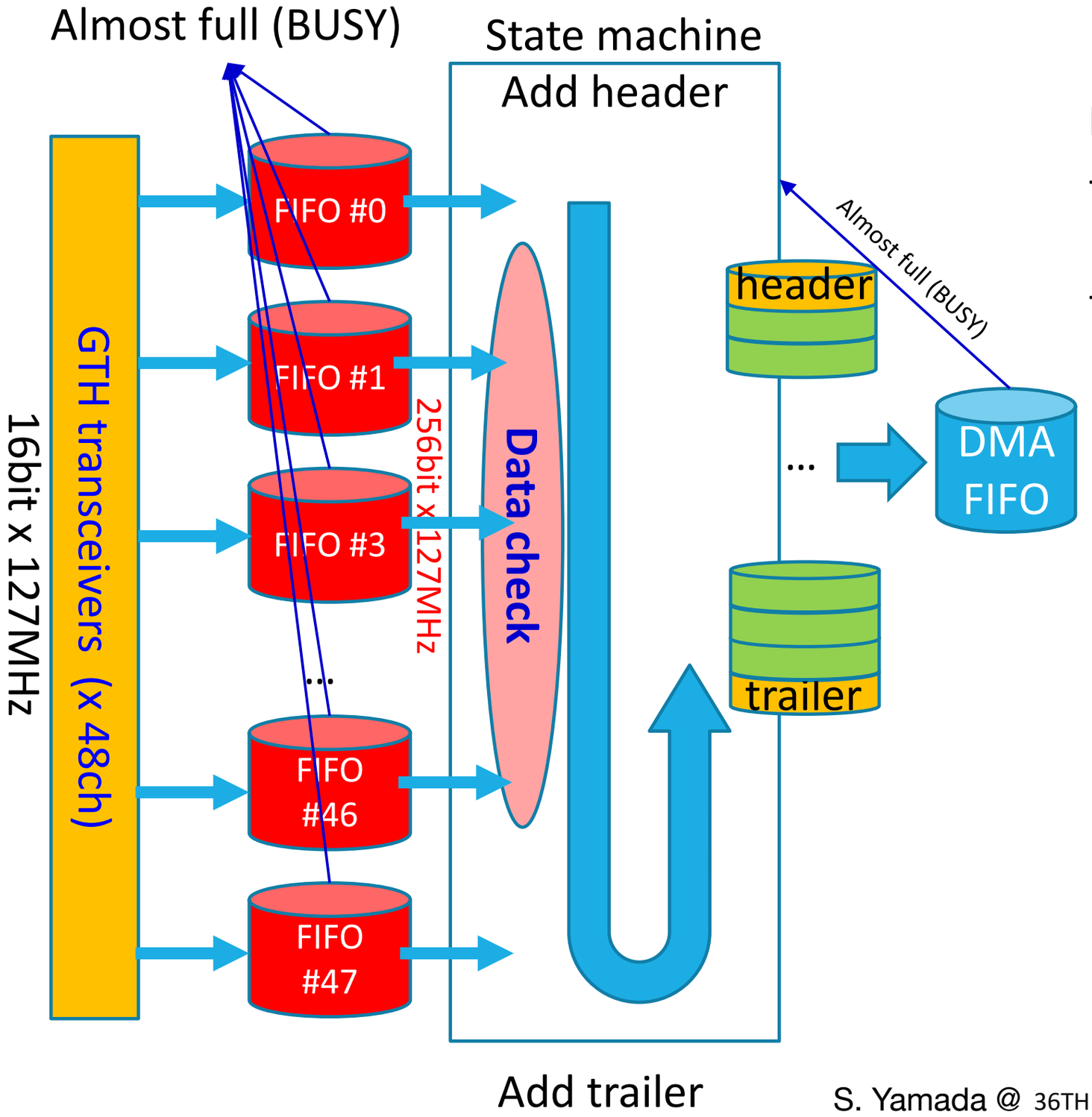


- Intel IP with external custom DMA controller
- Implemented as a QSYS module by Piotr Kapusta
- External DMA controller:
  - Extends DMA capabitilies (organize transfers into PC memory to ease handling by software)
- 2 buffers for events coming from user logic:
  - 32kB FIFO
  - 32kB memory necessary for DMA IP

P. Robbe @ 36th B2GM

- Pulse trigger rate: 470 kHz (times 8 kBytes)
- Data transmission rate: 39 Gbits/s
  - Readout PC using 10 Gbps Ethernet
- 10 % of event detect back-pressure.
- Pulse trigger rate: 260 kHz, 21 Gbits/s, no event lost.

Userlogic: event building & formatting



Event-building -> O.K.

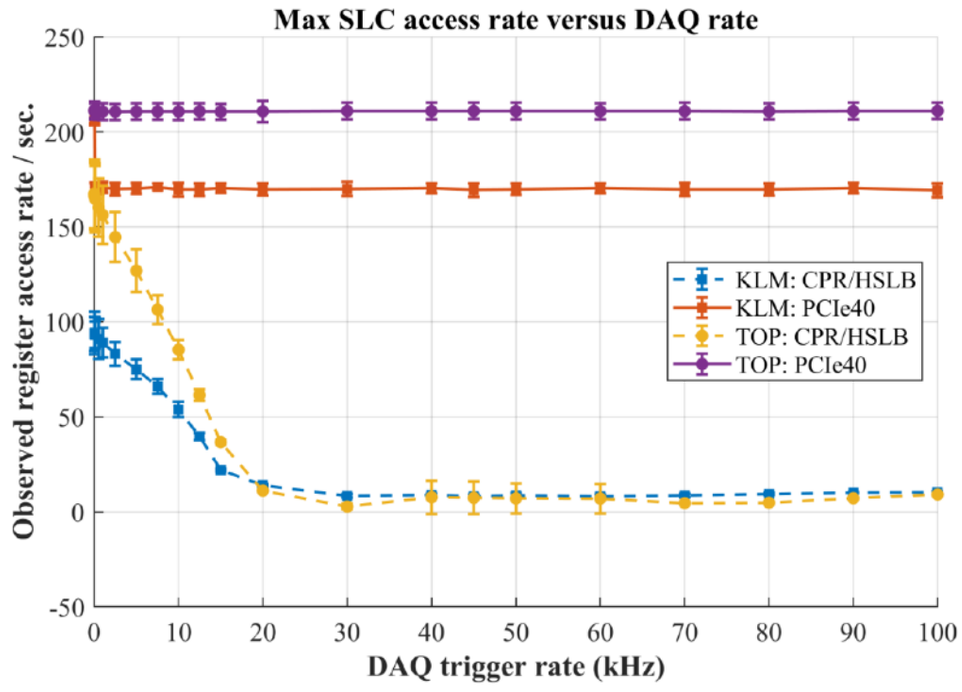
- Reduction of redundant info.
  -> O.K.
- Data-check -> to be done
  - CRC calculation
  - Event-incrementation
  - Mismatch in headers from different links

-> Add error-bit flag in an error event and later software will check only for error-flagged events.

Slow control performance

- 3 access methods of SLC for PCIe40 are fully working.
  - A7D8 and A16D32 kept the same feature as HSLB has
  - Streaming file separated based on packet length, which corresponding to KLM (6 words) and ARICH (100 words) specific functions.
- A16D32 access: 83 us / pre access <—>1 ms / pre access for HSLB
- Parallel access with multiple links is working well
  - It takes the same time for the access w/ and w/o parallel access
- Streaming file: 360 KBps for KLM method (6 words pre packet), 350 KBps for HSLB
- 1-2 sec downloading ARICH firmware by PCIe40, almost same as HSLB

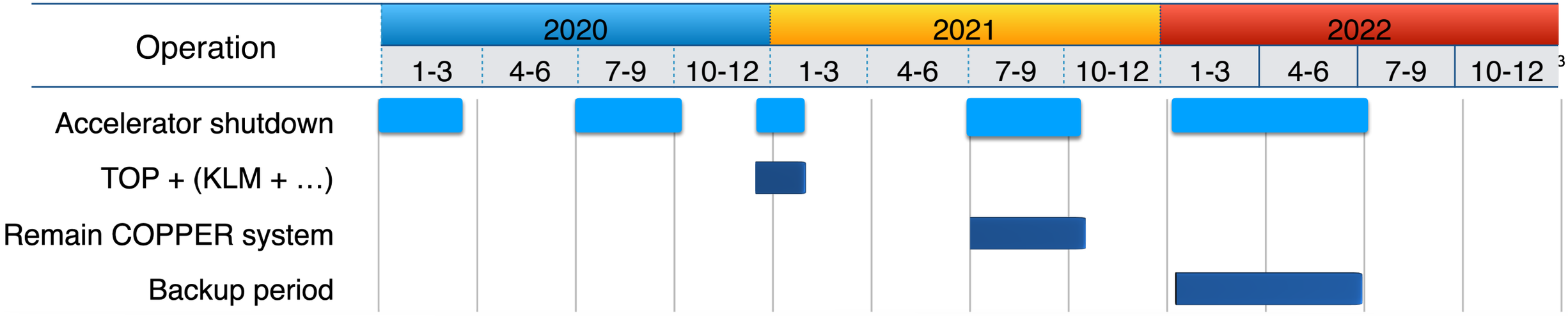
Detector	A7D8	A16D32	byte stream
SVD	○		
CDC		○	
TOP		○	
ARICH		○	○ (~3MB)
ECL	○	○	
KLM		○	○



Preparation for replacement

- **31 (24 + 7(M&O)) boards has been produced, then tested at CERN, they already arrived at KEK in Sep. 2020**
- **4 boards were installed in the serves for TOP and KLM replacement**
- **10 GbE NIC installed to ROPC, 10 GbE network switch <—> B3 HLT sever room installed**

Full replacement timescale



Current COPPER system will be on standby for a while after the installation, In case of a serious trouble, we can rollback to the COPPER system quickly

Summary

- Belle II DAQ system was designed to handle 40 times larger luminosity than the former Belle experiment
- A unified readout system was designed based on COPPER module for common readout of sub-detectors (except PXD)
- Region Of Interest (ROI) is used to reduce PXD data (1/10)
- 9 HLT units (3000 cores) is now operating during 2020ab, HLT reduce the data size by 1/3
- Operation with current DAQ system has been improved and data-taking efficiency reach to 84.2 % during 2020ab. still have room to be improve.
- COPPER cpu freeze and link errors (belle2link, b2ttlink) are the main issues in 2020ab for DAQ

- Pcie40 module is adopted for the upgrade of Belle II DAQ readout system
- Upgrade will keep the main feature of current readout system to keep the modification of sub-detectors as less as possible.
- Firmware and software development are almost done
- Replacement is scheduled this winter for TOP and KLM, the others are during summer shutdown 2021.