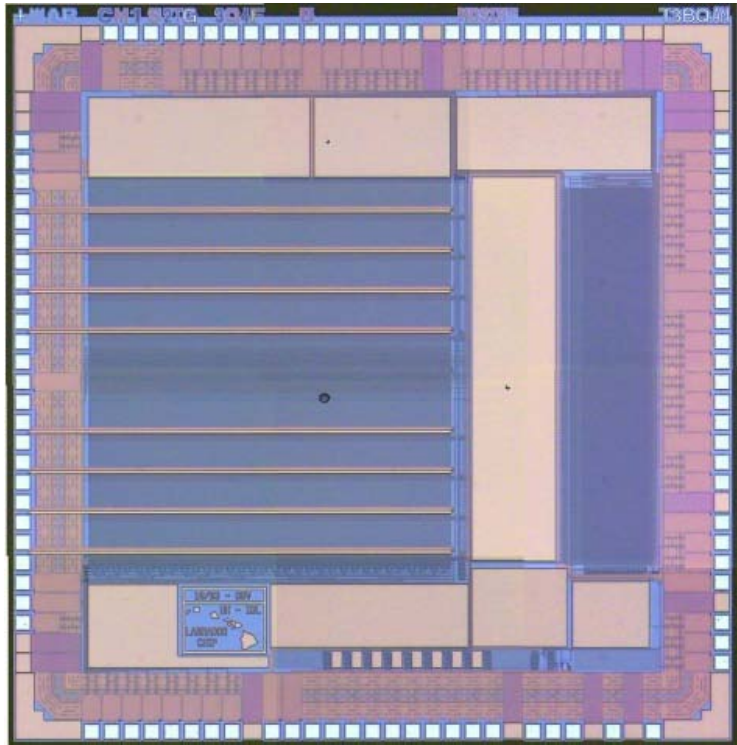


The "Giga" Era of Instrumentation at the Discovery Frontier



Gary S. Varner

University of Hawai'i

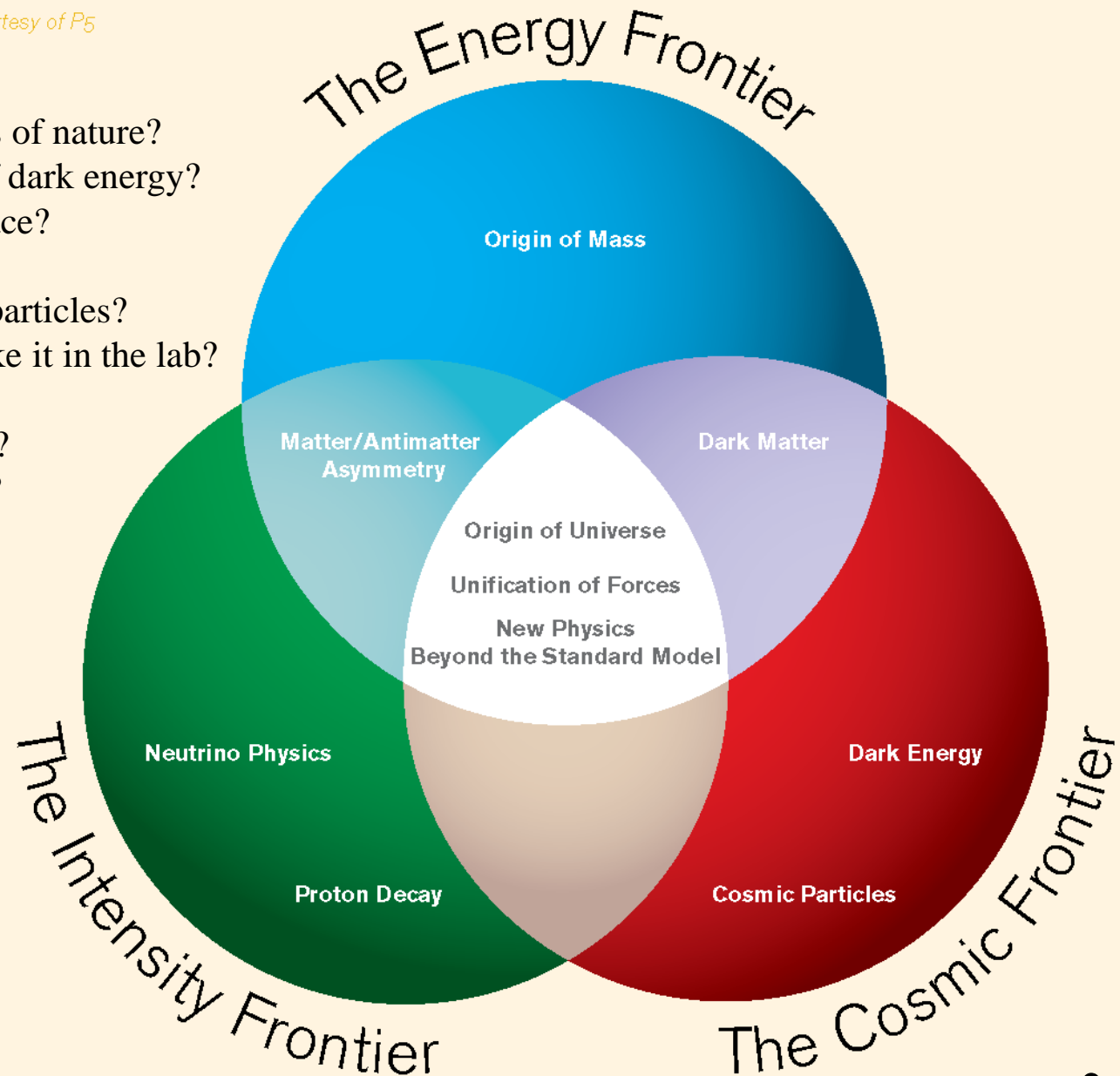
KMI Seminar, Nov. 9, 2012



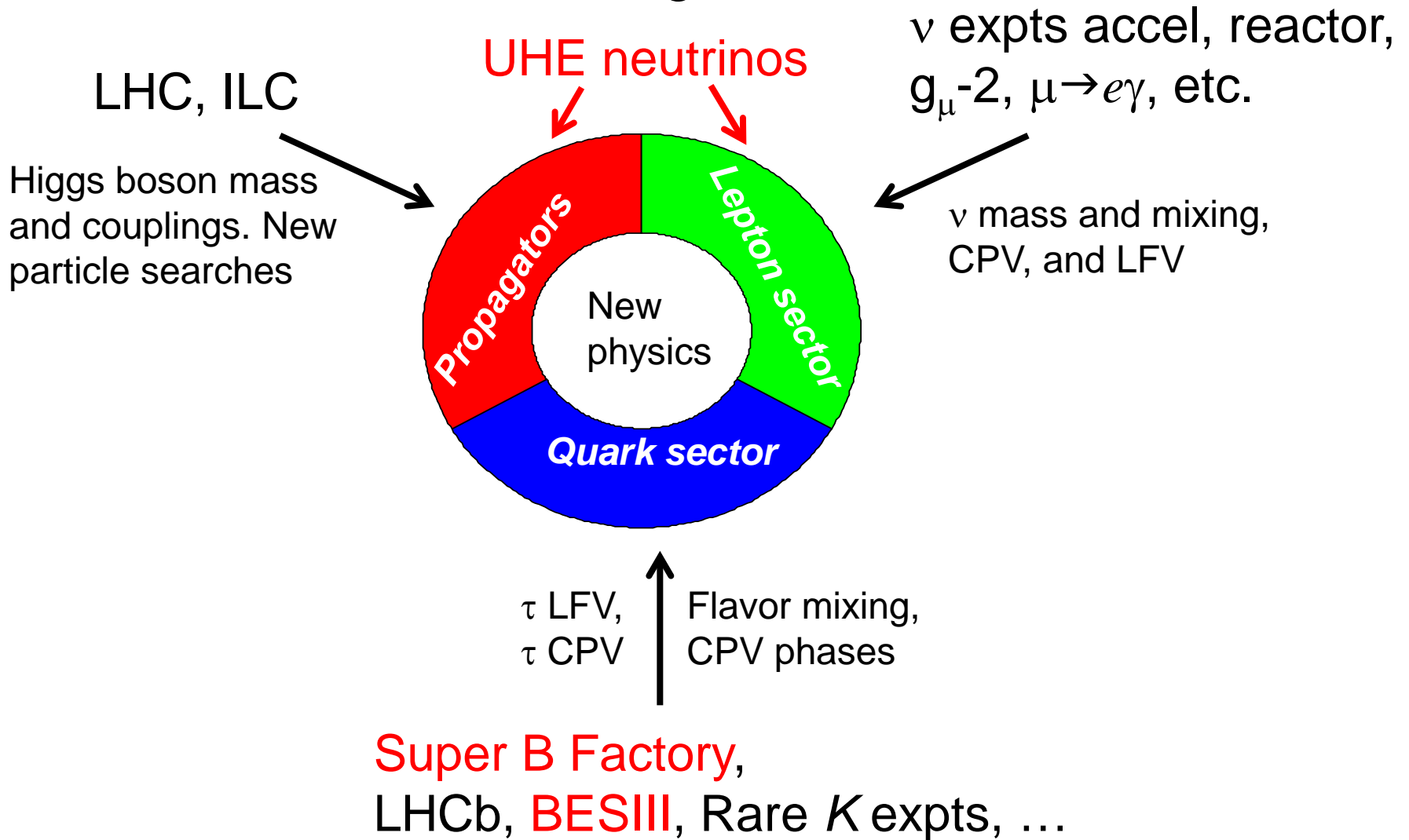
The big Questions

Diagram courtesy of P5

1. Are there undiscovered principles of nature?
2. How can we solve the mystery of dark energy?
3. Are there extra dimensions of space?
4. Do all the forces become one?
5. Why are there so many kinds of particles?
6. What is dark matter? Can we make it in the lab?
7. What are neutrinos telling us?
8. How did the universe come to be?
9. What happened to the antimatter?



The (Particle Physics) Discovery Frontier



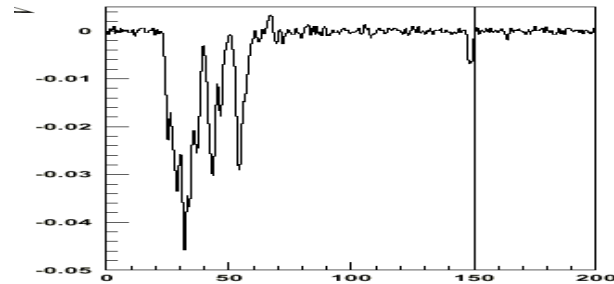
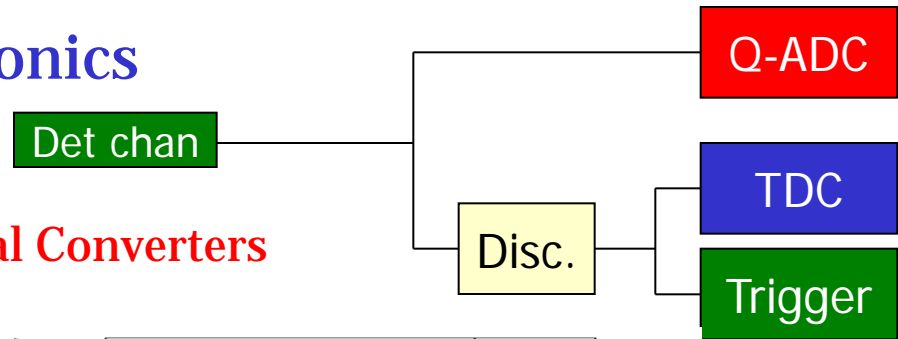
Overview

- Further advances at the Discovery Frontier
 - Depends upon developing new instruments and techniques
 - Exploit commodity resources
- The “easy” experiments are being completed
 - Can’t necessarily scale up ($\text{\$}\text{\$}\text{\$}$, $T > N * t_{\text{gradstudent}}$)
 - Innovation fuels new opportunities
- What I hope to convey:
 1. What the “Giga” Era means
 2. Key elements
 3. An example where this has been fundamentally enabling
 4. The Belle II (Time Of Propagation) Particle Detector

Detector Instrumentation Evolution

- Traditional “crate based” electronics

- Gated Analog-to-Digital Converters
- Referenced “triggered” Time-to-Digital Converters

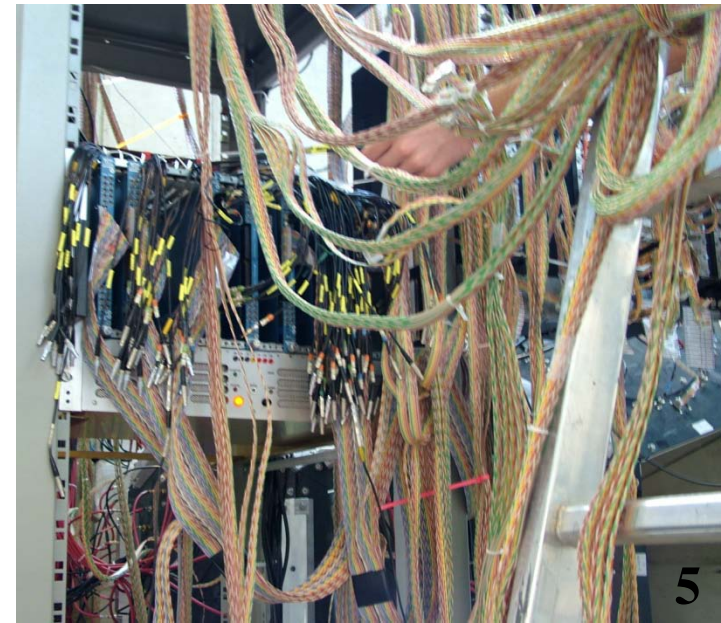
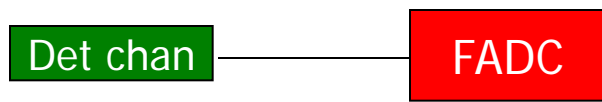


- High-rate applications

- “pipelined operation”
- Low-speed, low-resolution sampling

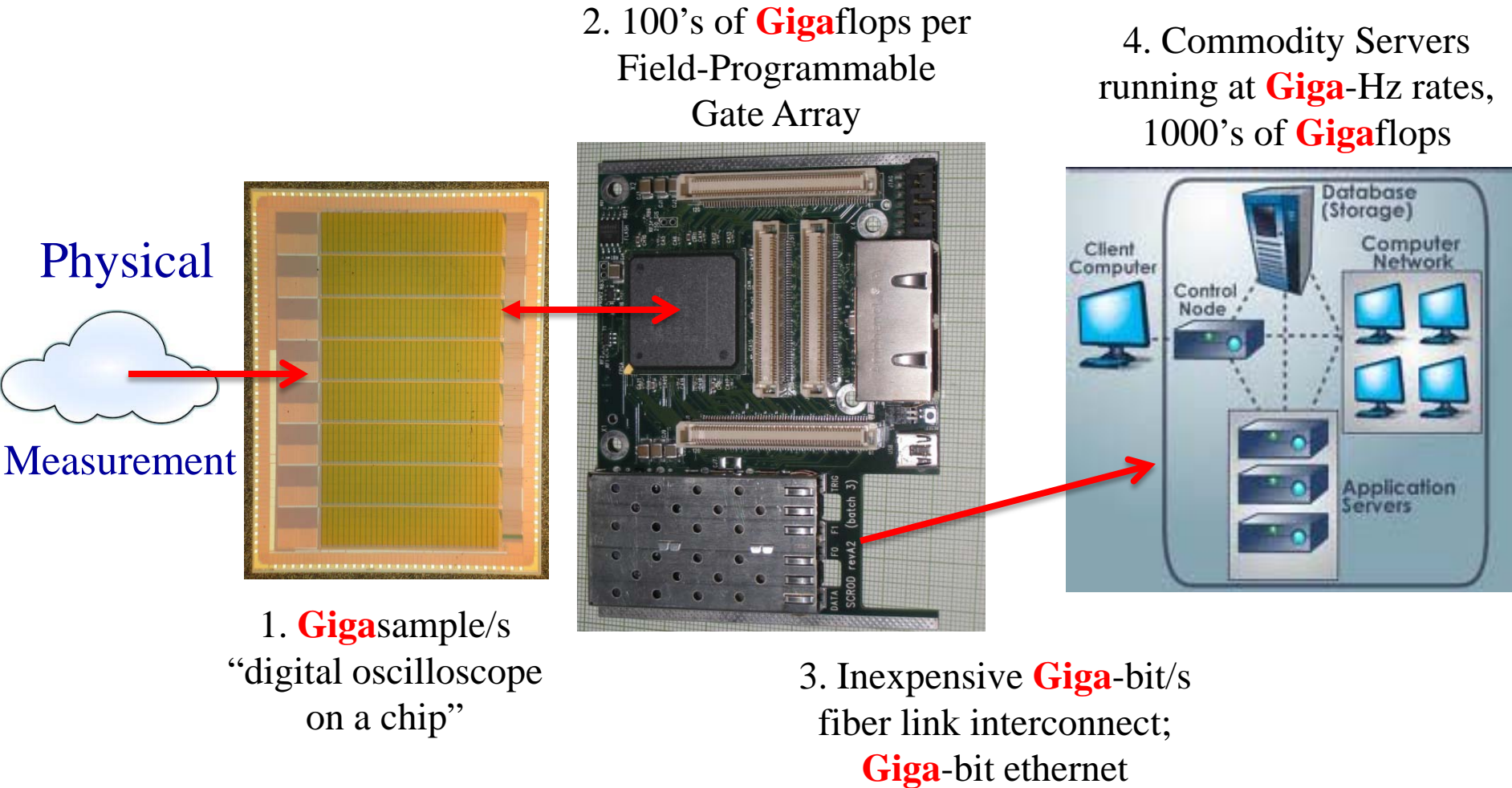
- High channel counts

- Motivation to reduce cabling
- Integrate electronics onto detector elements



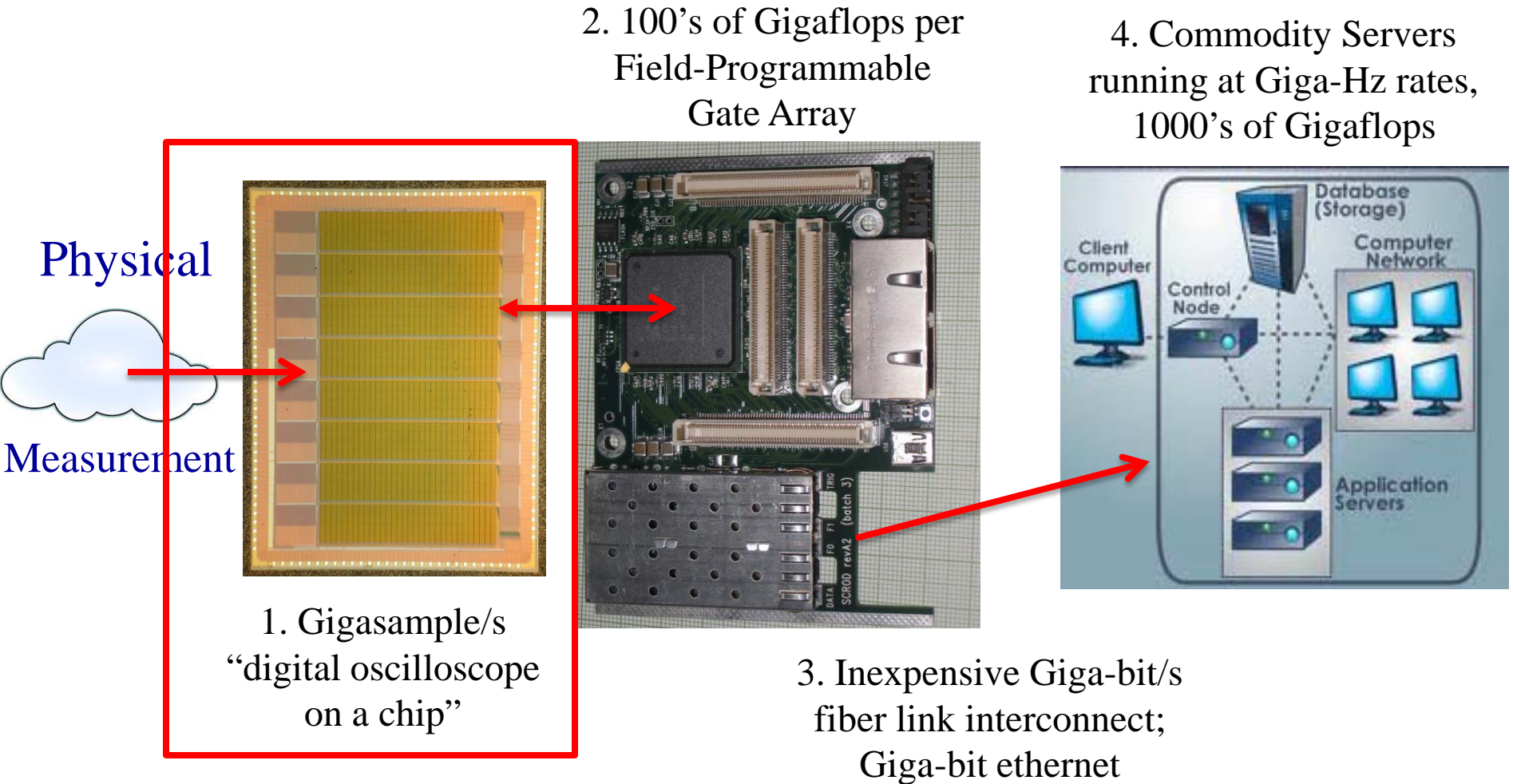
Issues: cost, power, resolution, data volume

A "Giga" Overview (Modern Readout)



Technology advances → high rate, high-precision experiments

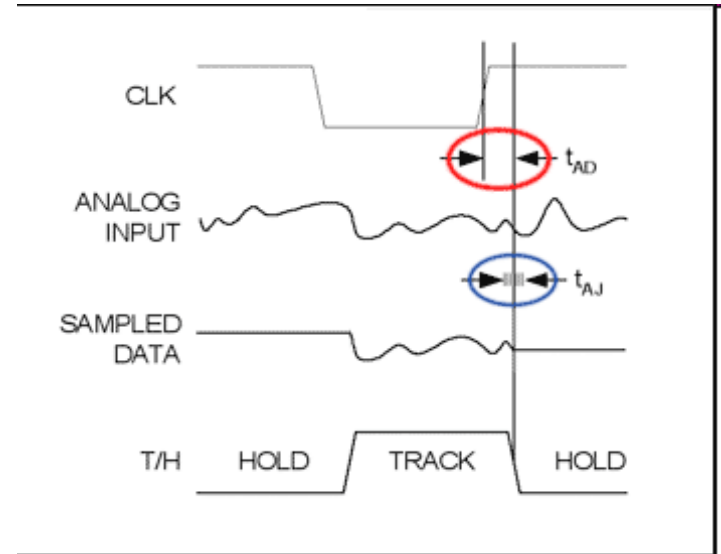
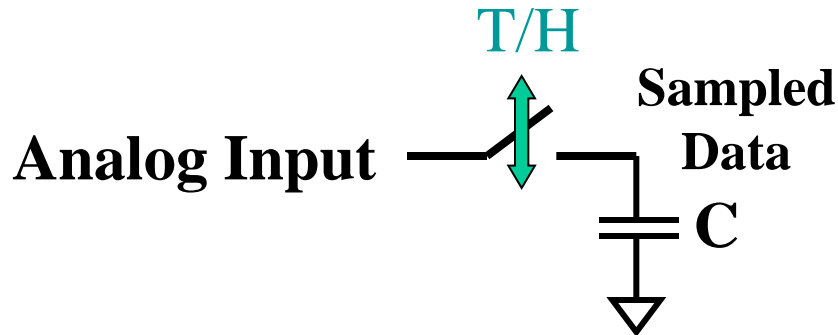
Focus on the first of these



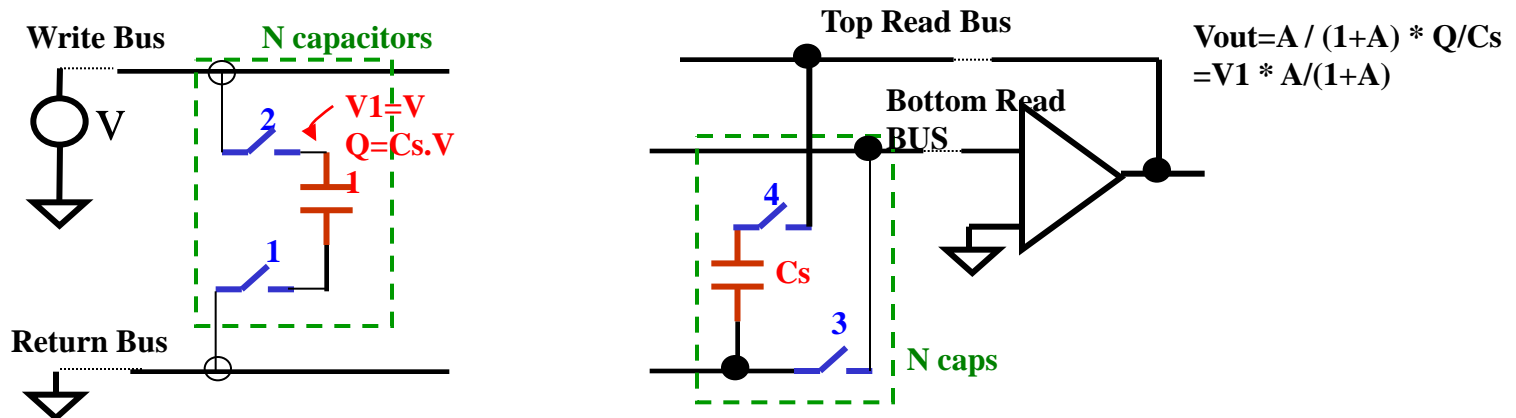
- Defines limit of the physical measurement
- What Instrumentation Physicists contribute

Underlying Technology

- Track and Hold (T/H)

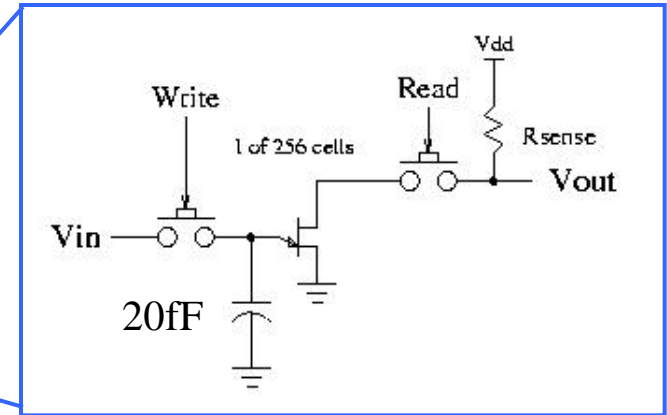
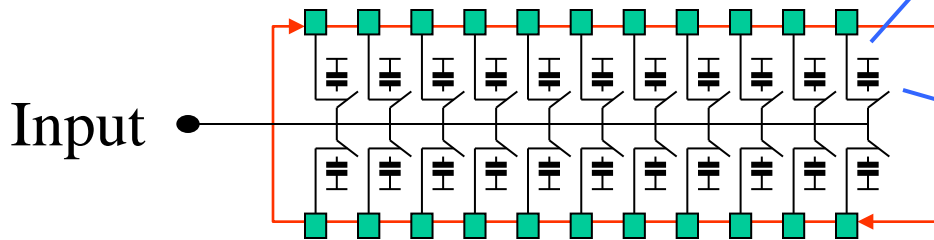


- Pipelined storage = array of T/H elements, with output buffering



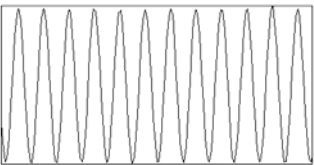
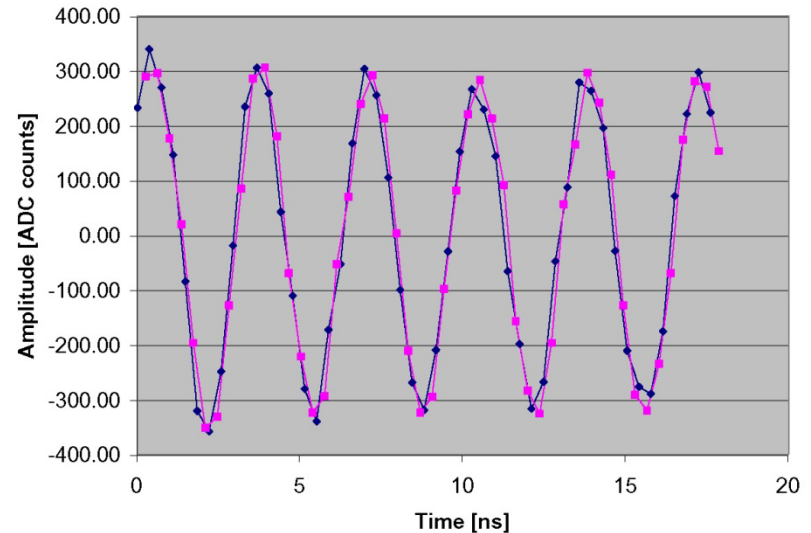
Switched Capacitor Array Sampling

- Write pointer is ~few switches closed @ once

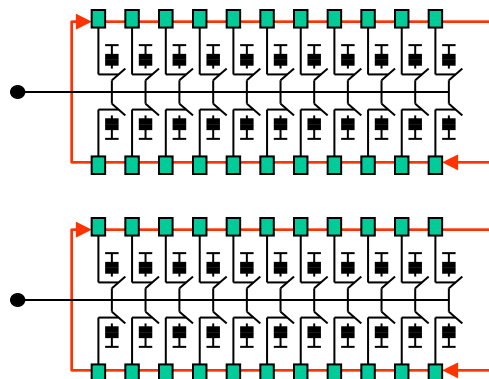


Tiny charge: $1\text{mV} \sim 100e^-$

300MHz RF Sine [50mV amplitude]



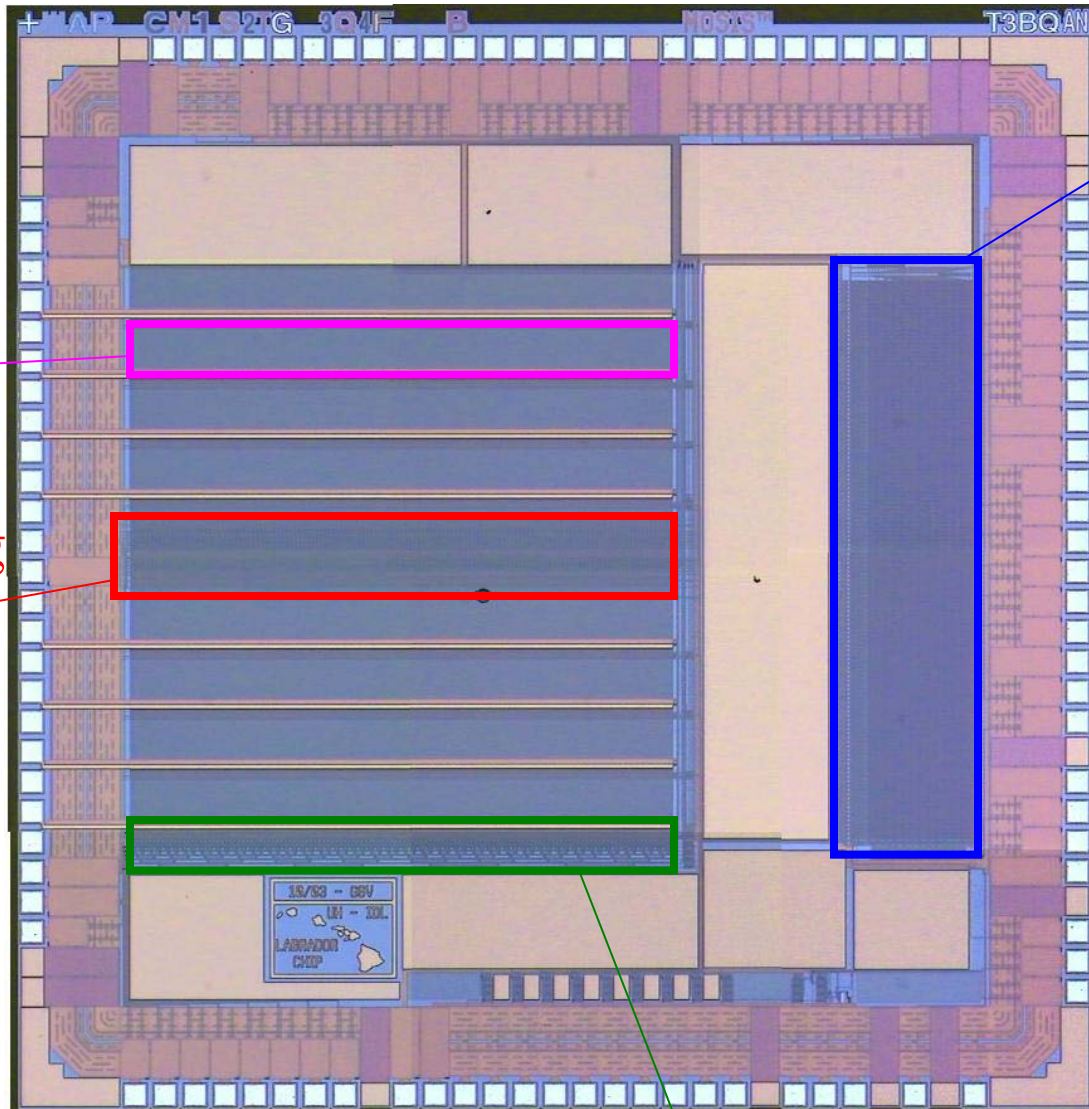
Few 100ps delay



Channel 1

Channel 2

Basic Functional components



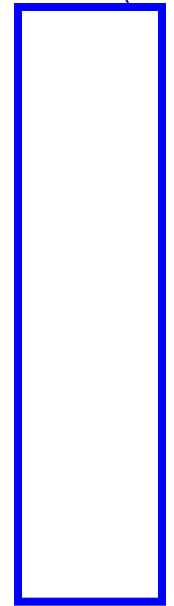
Single storage
Channel

Sample timing
Control

Few mm x
Few mm
in size

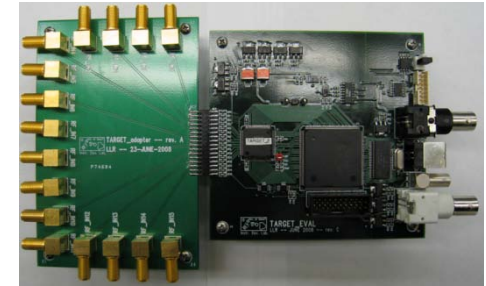
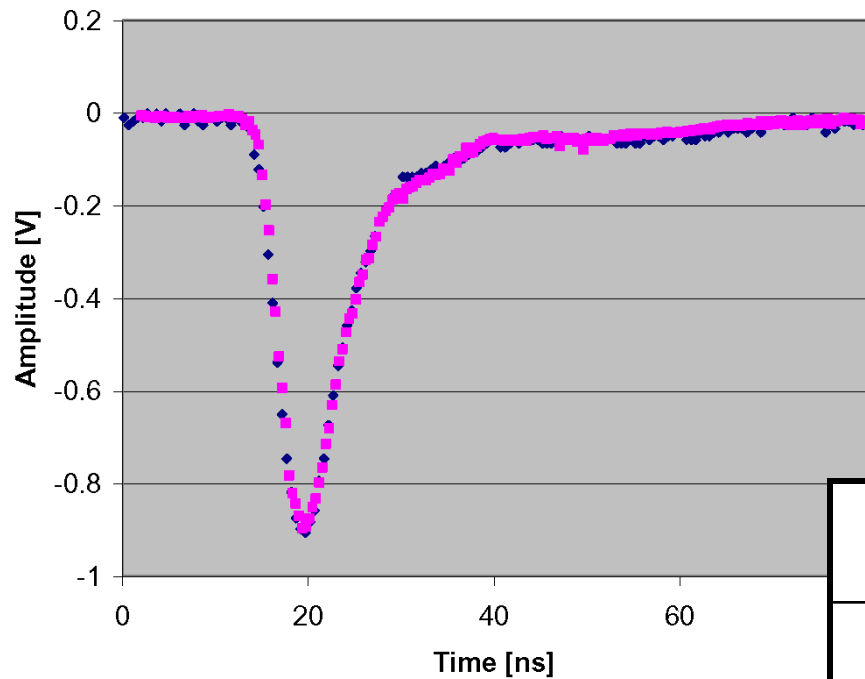
Readout Control

On or off-
chip ADC



The Giga Package

PMT pulse comparison



- 2 GSa/s, 1GHz ABW
- Tektronics Scope
- 2.56 GSa/s LAB

“oscilloscope on a chip”

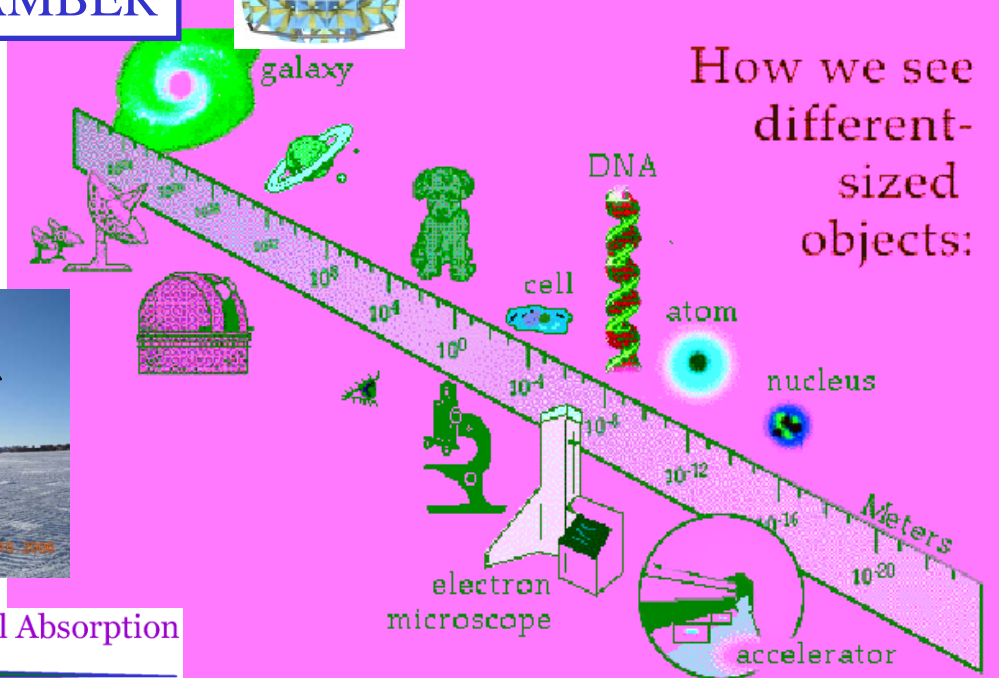
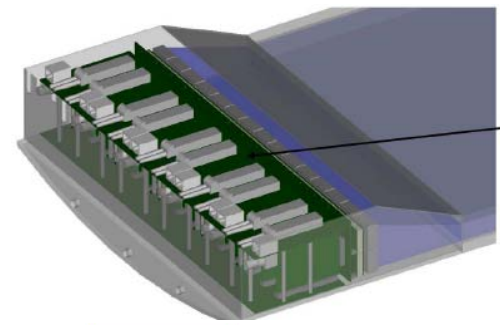
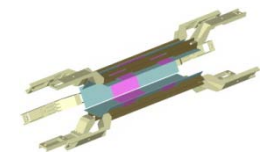
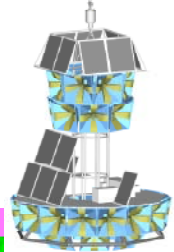


	WFS ASIC	Commercial
Sampling speed	0.1-6 GSa/s	2 GSa/s
Bits/ENOBs	16/9-13+	8/7.4
Power/Chan.	$\leq 0.05W$	Few W
Cost/Ch.	$< \$10$ (vol)	$> 100\$$

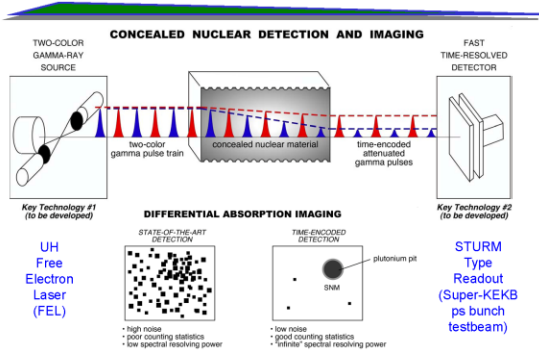
Very broad Impact



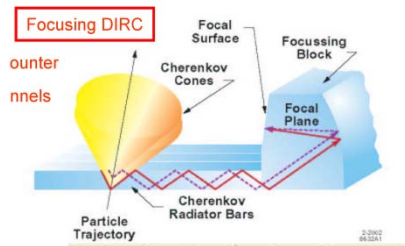
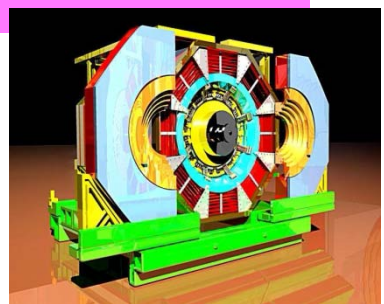
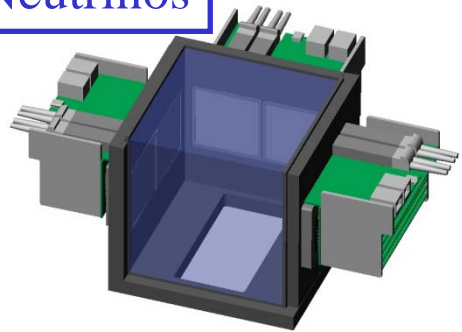
AMBER



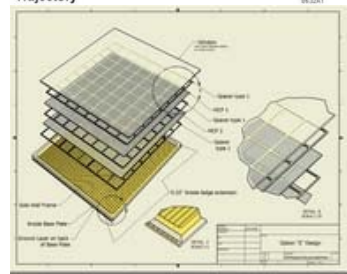
Time-Encoded Differential Absorption



Neutrinos

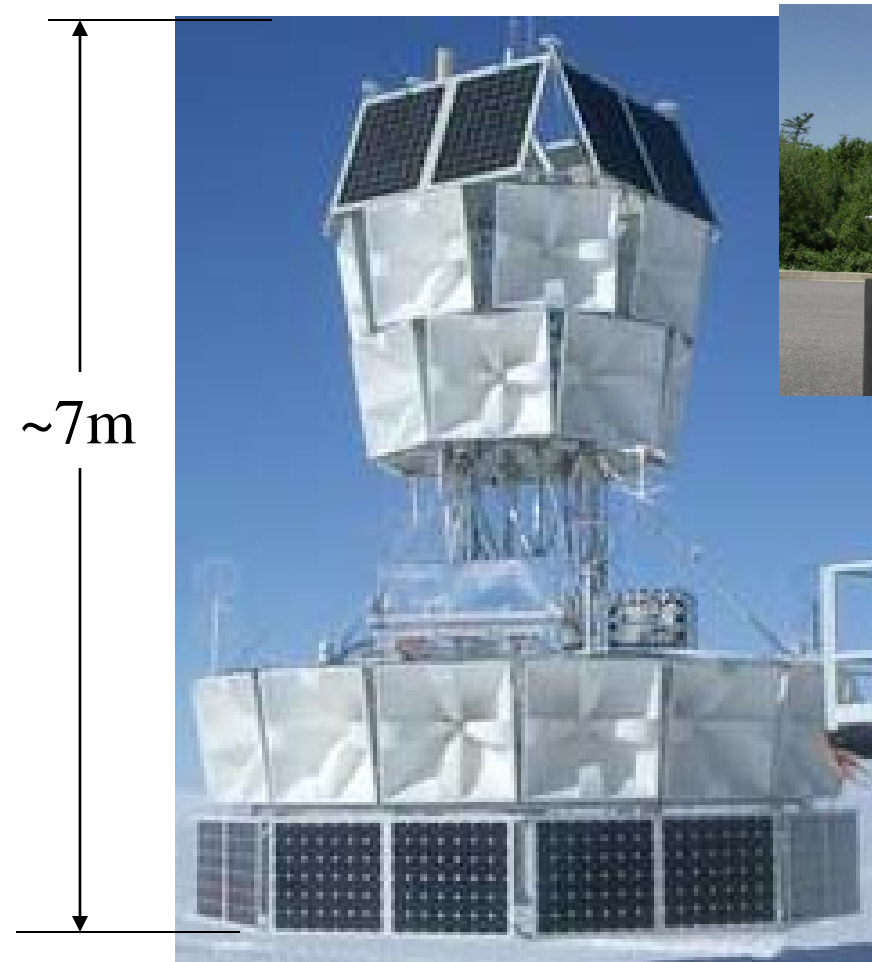


LAPPD →

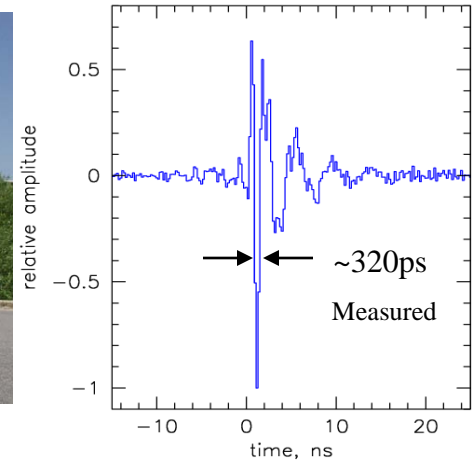


Fundamental enabling technology (all current Hawaii activities)

To be explicit, a demanding Application

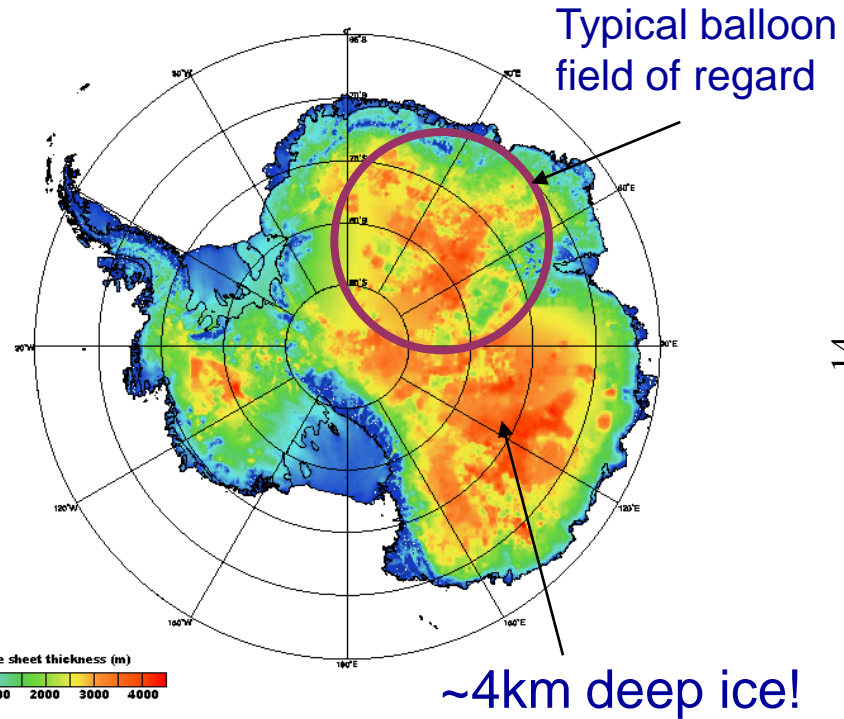
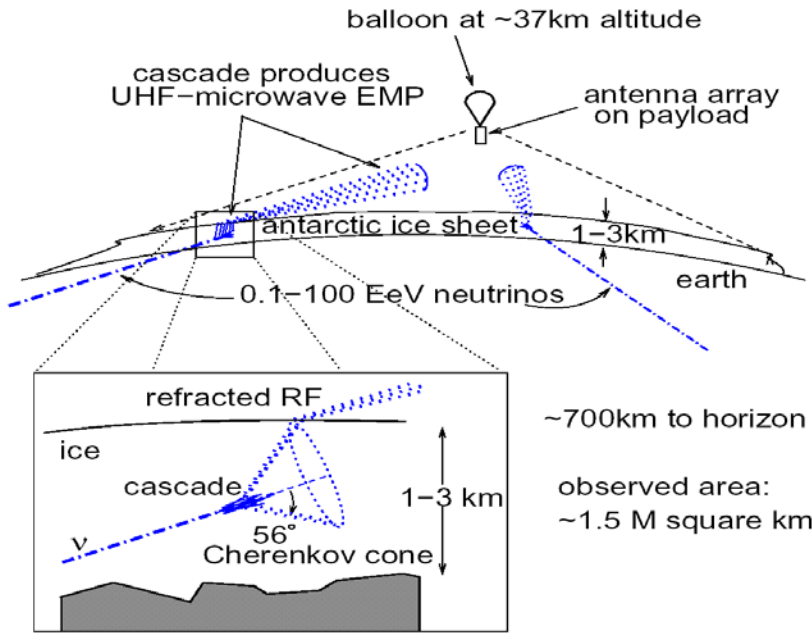


Antarctic Impulsive Transient Antenna
(ANITA-I)

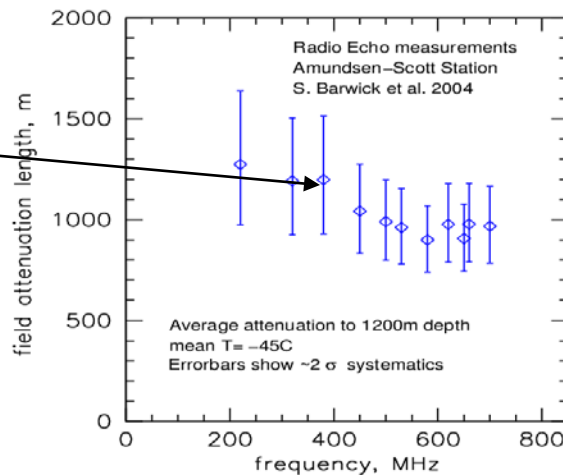


- RF Transient (impulsive) Events (200-1200 MHz)
- 324 chan. @ 2.6GSa/s
- **Completely solar powered** (tight demands on power, few hundred W total)
- Need full waveforms

ANITA concept



Ice RF clarity:
~1.2km(!)
attenuation length



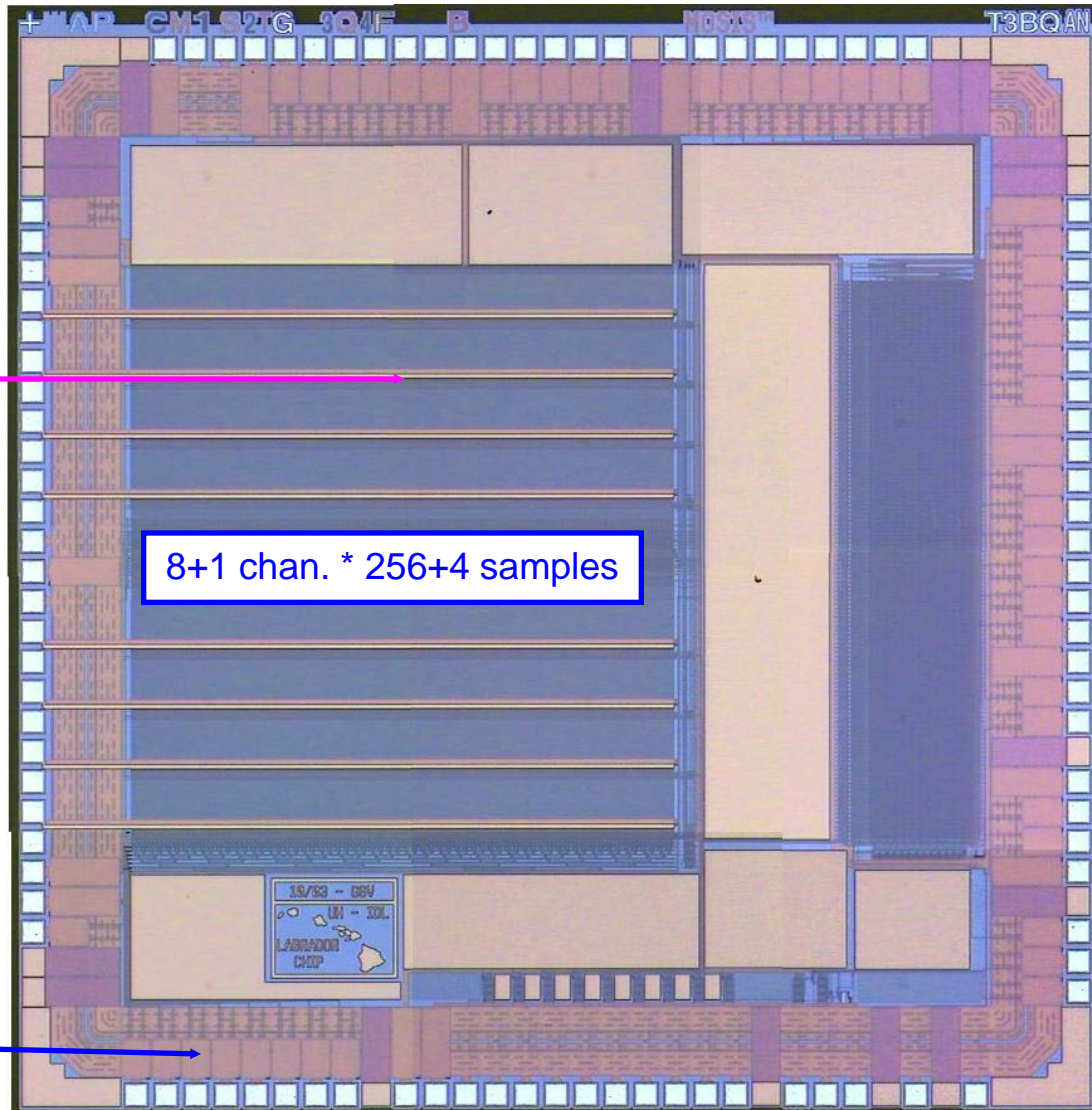
Effective “telescope” aperture:

- ~250 km³ sr @ 10¹⁸ eV
 - ~10⁴ @ km³ sr 10¹⁹ eV
- (compare to ~1 km³ at lower E)

Large Analog Bandwidth Recorder and Digitizer with Ordered Readout [LABRADOR]

Straight Shot RF inputs

- Switched Capacitor Array (SCA)
- Massively parallel Wilkinson ADC array



- Common STOP acquisition
- 3.2 x 2.9 mm
- Conversion in 120 μ s (all 2340 samples)
- Data transfer takes 80 μ s
- Ready for next event in 200 μ s

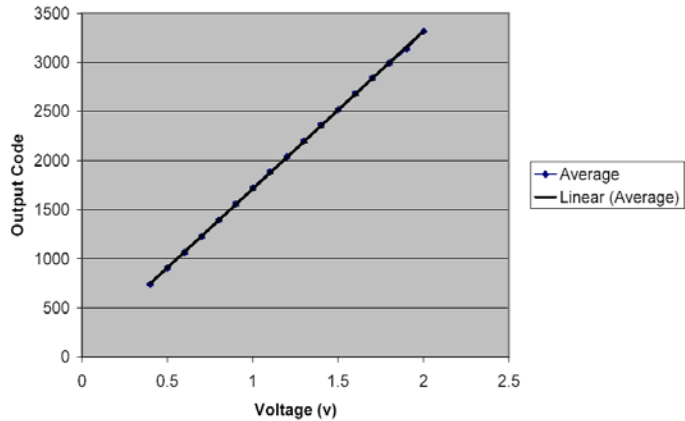
Random access:

LABRADOR performance

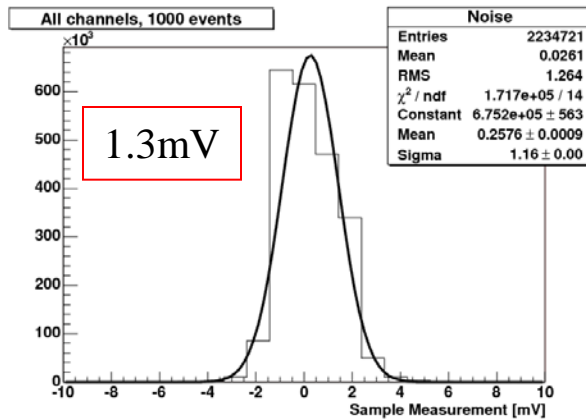
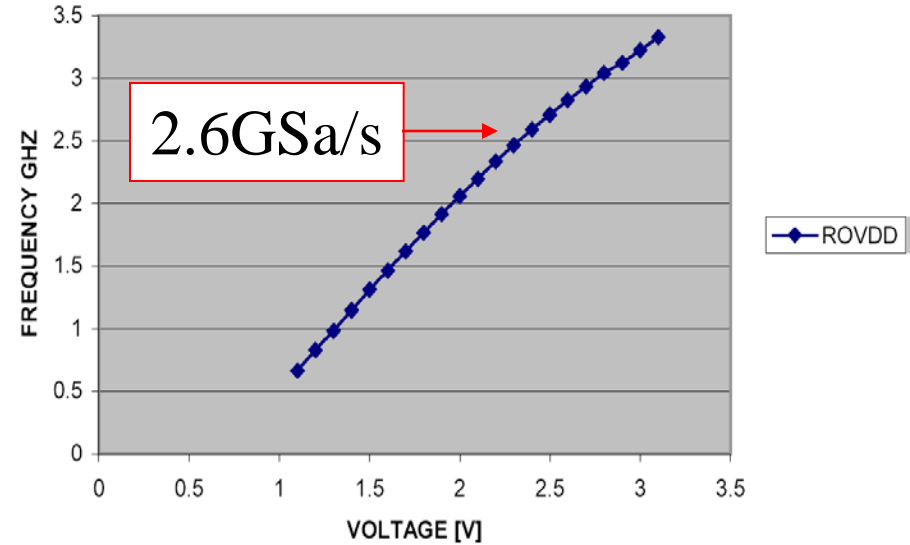
12-bit ADC

Labrador ADC Performance

$$y = 1606.8x + 105.26$$
$$R^2 = 0.9999$$



LABRADOR SAMPLING FREQUENCY (ROGND)

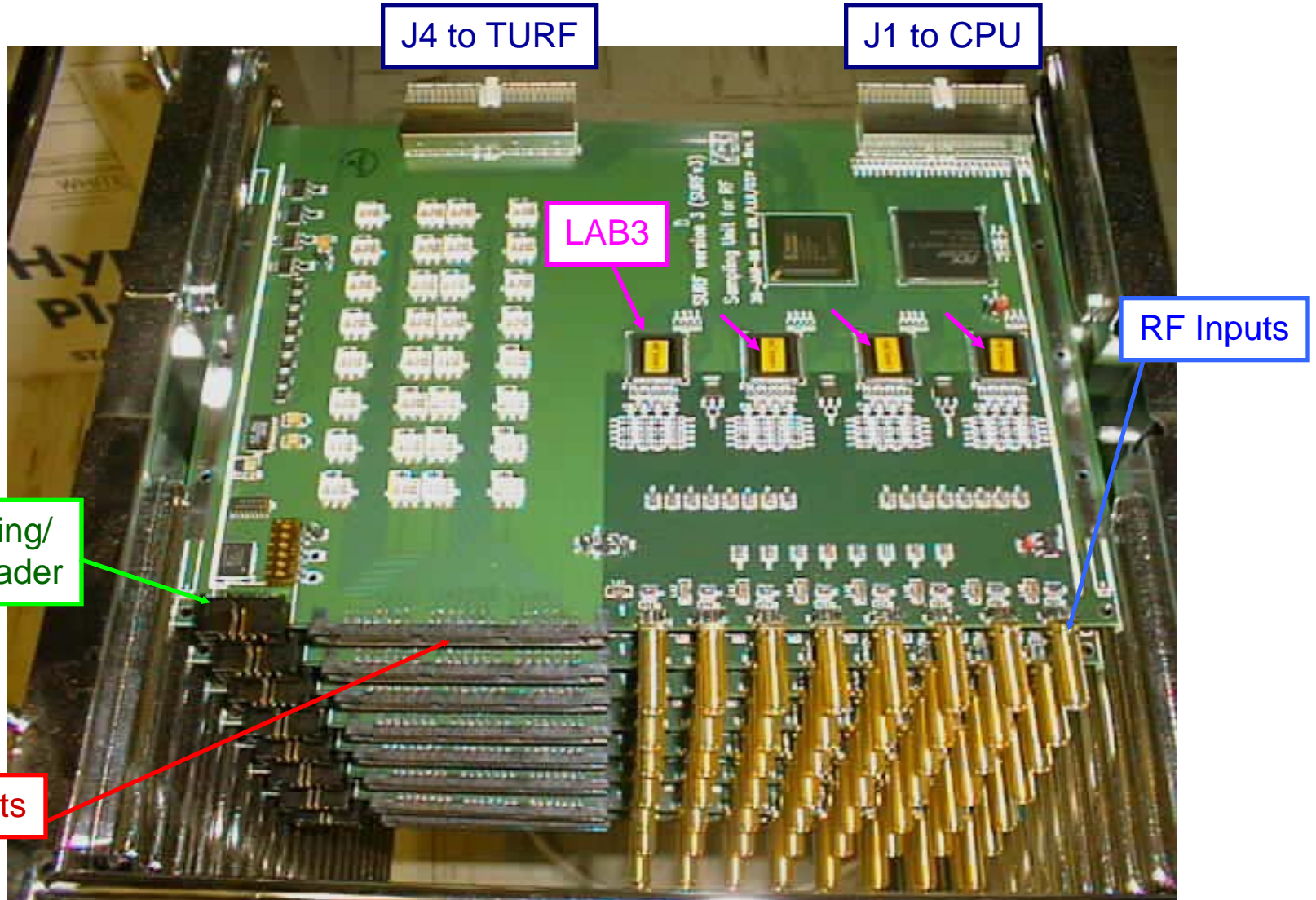


- 10 real bits (1.3V/1.3mV noise)
- Excellent linearity, noise
- Sampling rates up to 4 GSa/s with voltage overdrive

SURFv3 Board

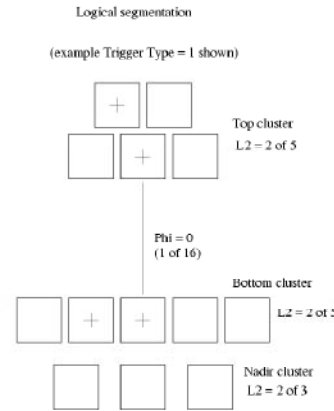
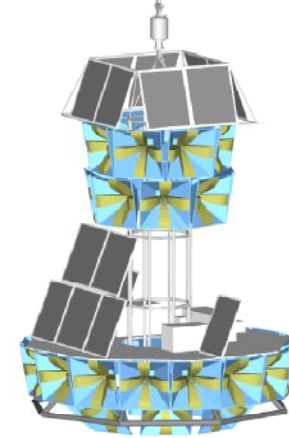
(SURF = Sampling Unit for RF)

(TURF = Trigger Unit for RF)

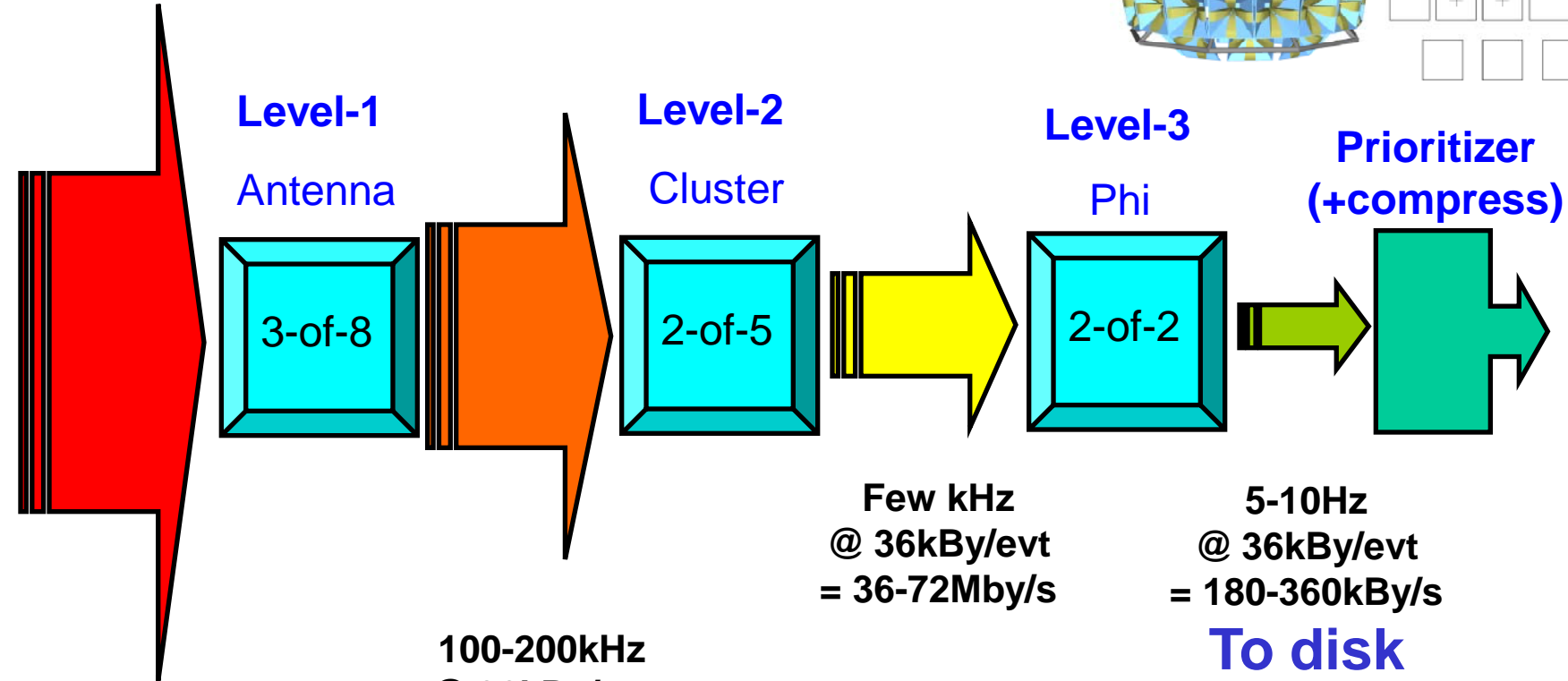


PCI bus: 64bits, 66MHz ~ 0.5 GigaByte/s (upgrading for 3rd flight)

A "high rate" Experiment



Raw Signals



80 RF channels
@ 1.5By * 2.6GSa/s
= 312 Gbytes/s

100-200kHz
@ 36kBy/evt
= 3.6-7.2Gby/s

Few kHz
@ 36kBy/evt
= 36-72Mby/s

5-10Hz
@ 36kBy/evt
= 180-360kBy/s

To disk

Few events/min TDRSS

Permits thermal noise level operation

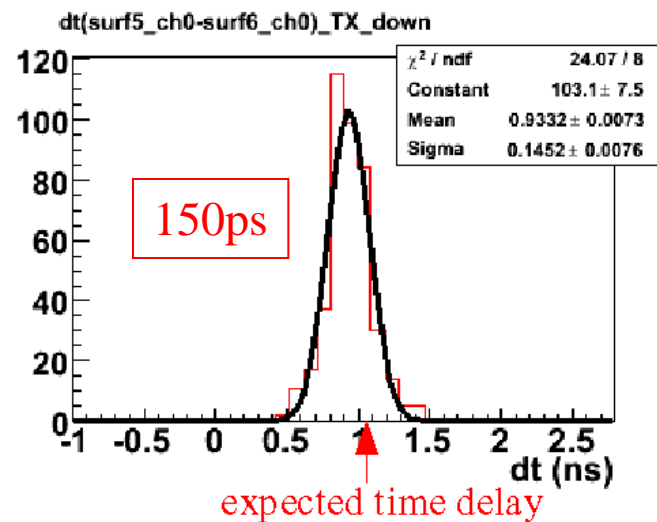
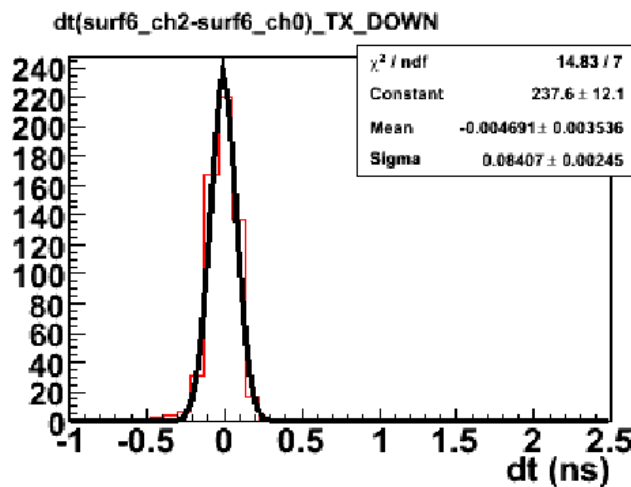
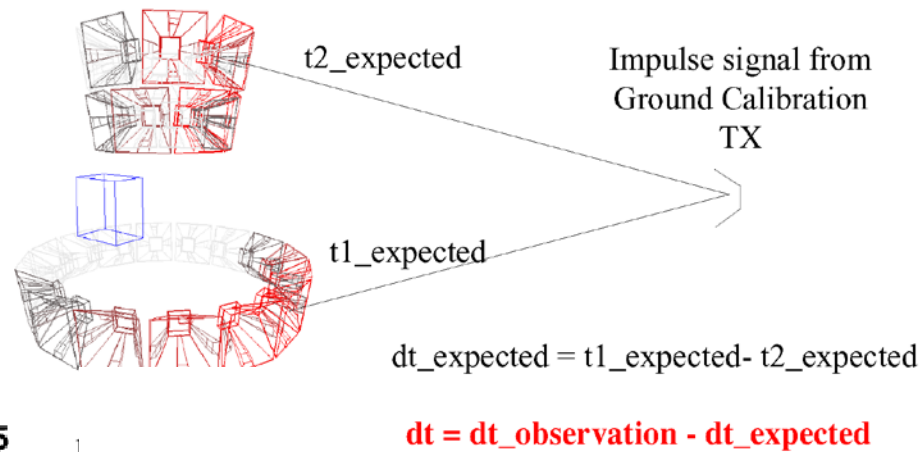
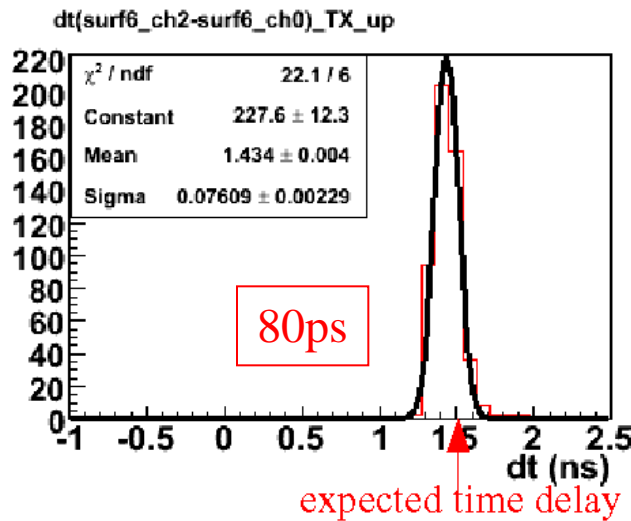
Timing vs Angle (with Impulse Calibration Radio Signal)

TX Up
by 1.56 m

Vertical Angle
Dependency

TX Down

Jiwoo Nam
UC Irvine



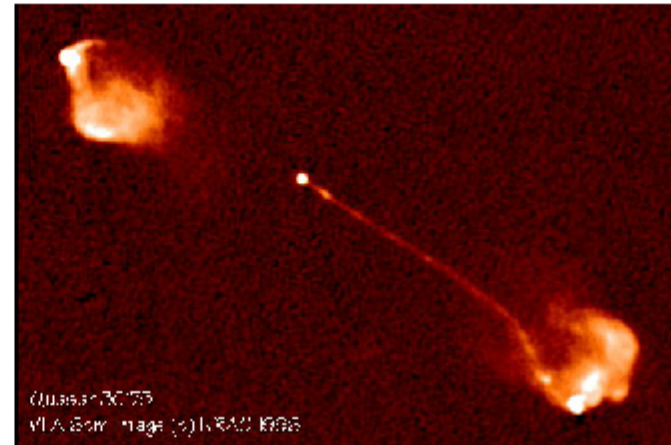
Face to TX ← Horizontal Angle Dependency → Off by 1 Antenna

Pulse Phase interferometry

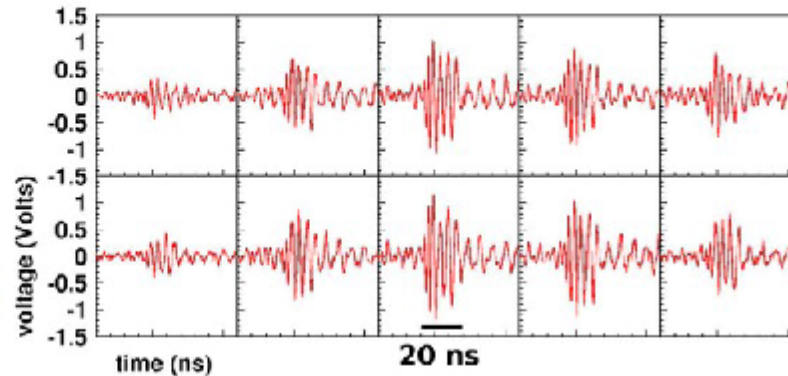
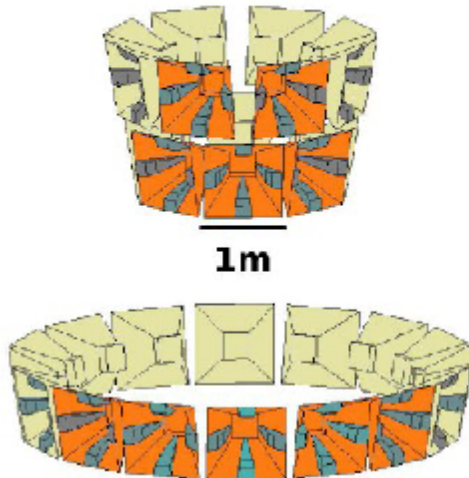
A. Romero-Wolf (Hawaii)

Ultrawide-band Interferometry

- Interferometric technique applied by radio astronomers.
- They use single narrow band frequency.
- More interested in source imaging rather than point source direction reconstruction.

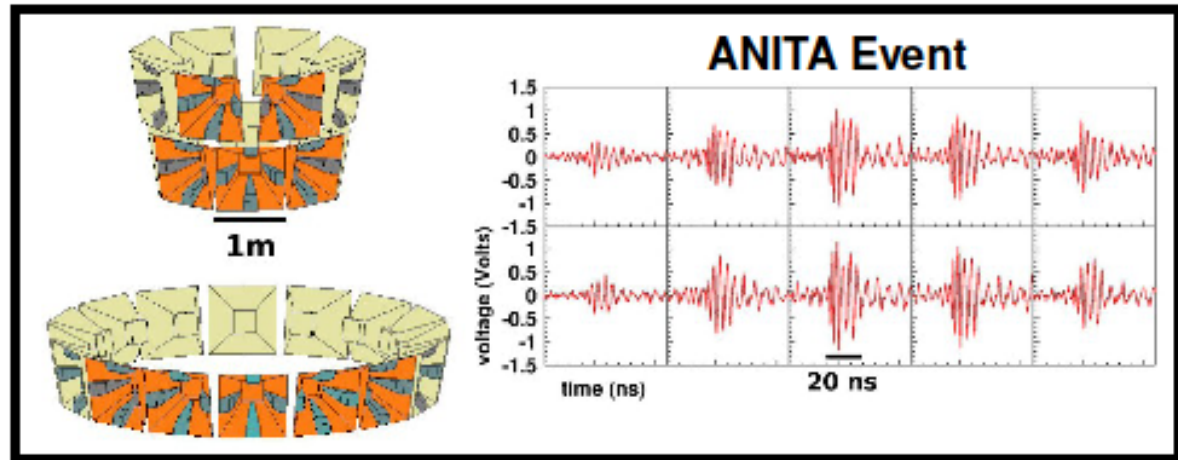


Produce Ultrawide-band Interferometric Images with ANITA

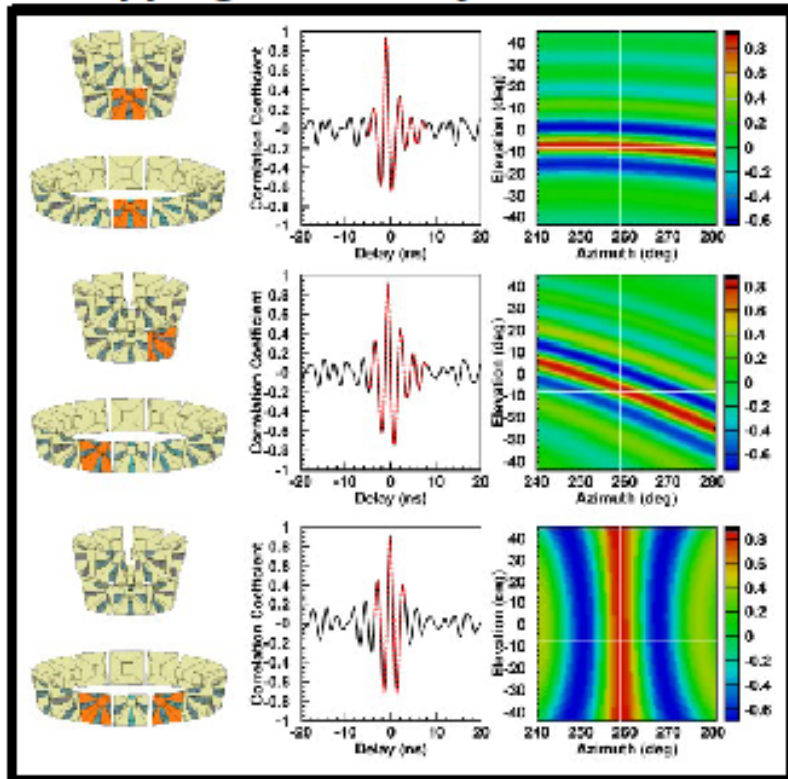


~30ps (16ps) resolution between channels

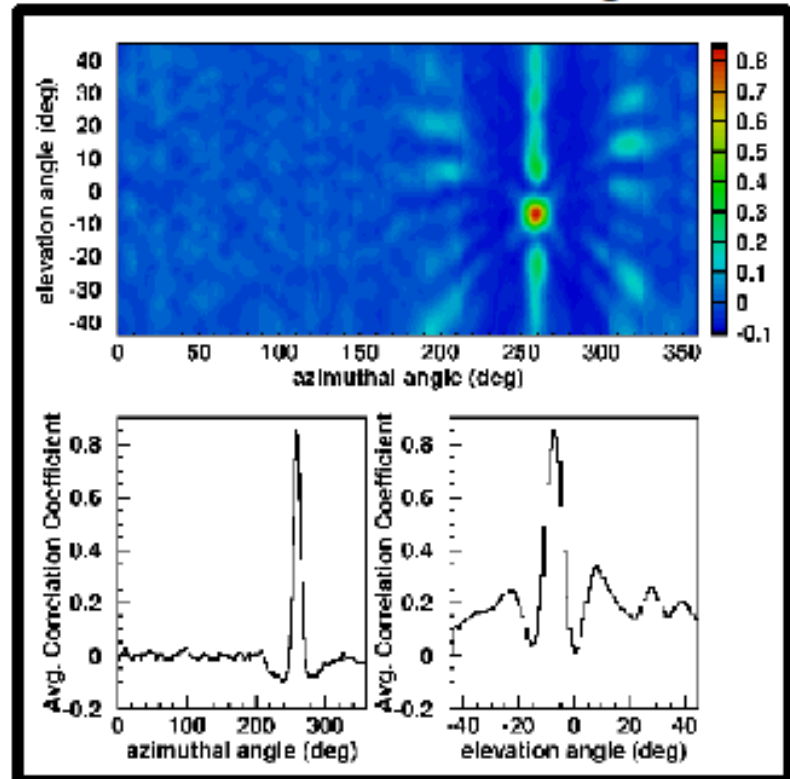
Mapping Waveforms to Interferometric Images



Mapping Time Delay Correlations



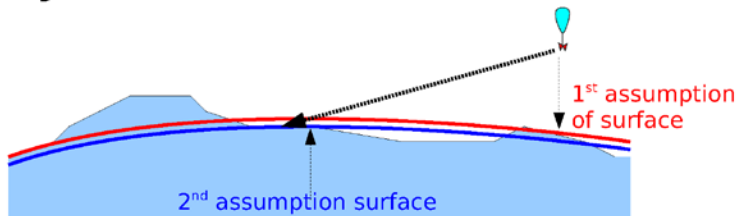
Interferometric Image



After full calibration – 100's km

<30ps timing

RF Projection onto the surface



Fast Algorithm: Line Sphere intersection

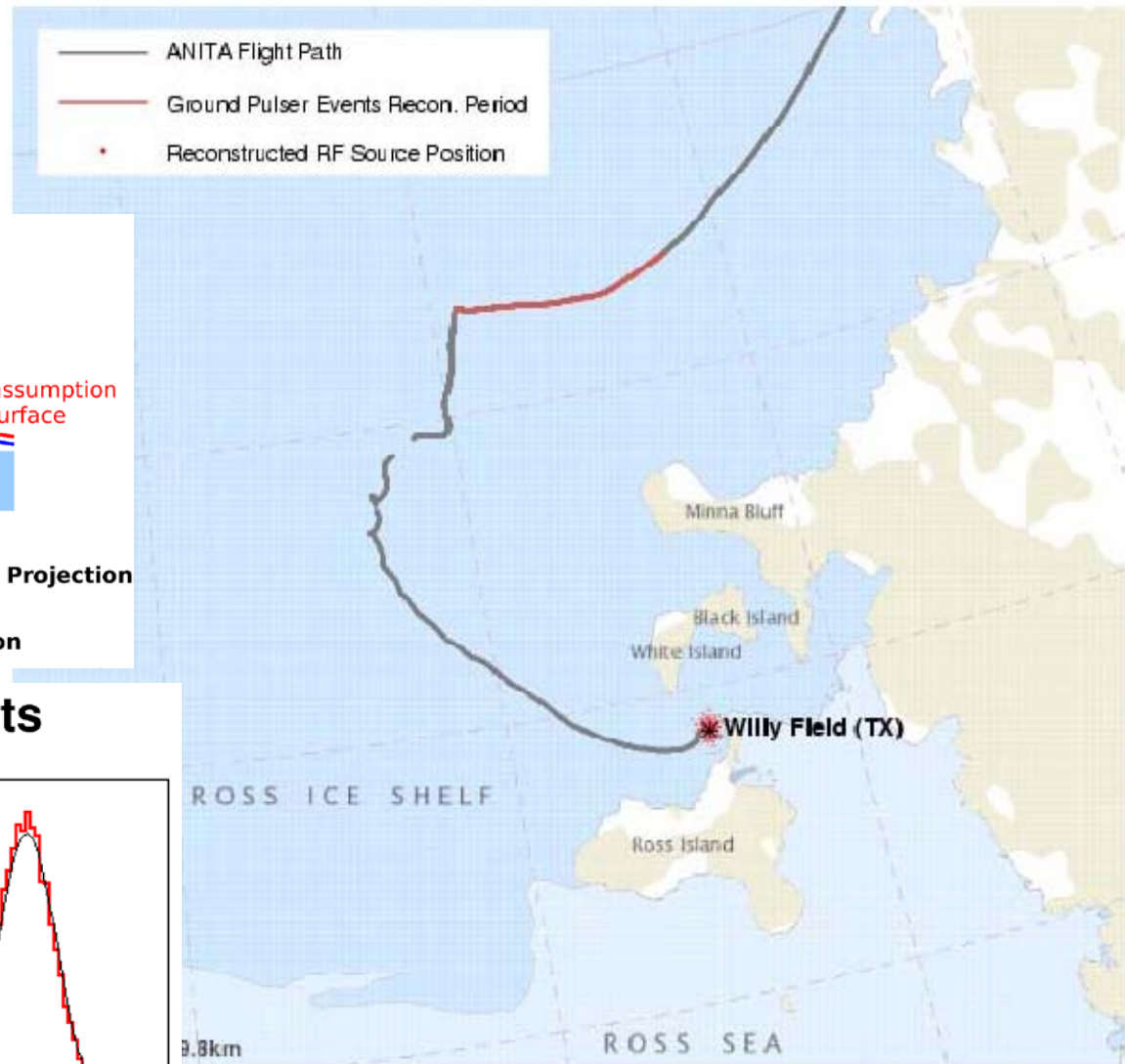
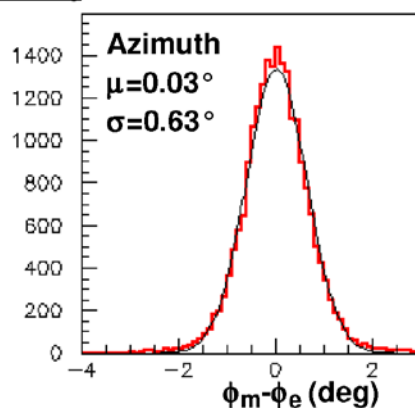
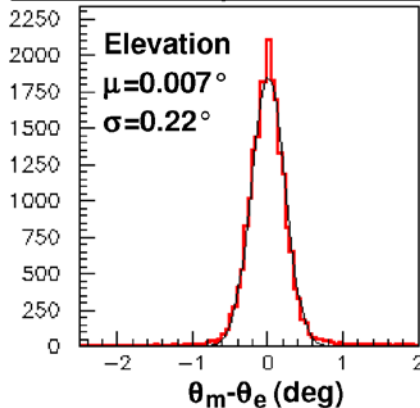
1st $R_{\text{earth}} = \text{Geoid} + \text{Surface} @ \text{Ballon position} \rightarrow \text{Rough Projection}$

2nd $R_{\text{earth}} = \text{Geoid} + \text{Surface} @ (\text{position from 1st})$

3rd: one more iteration \rightarrow converged after 2nd iteration

V-pol results

Borehole Data (used for calibrations)



The “no free lunch” Theorem

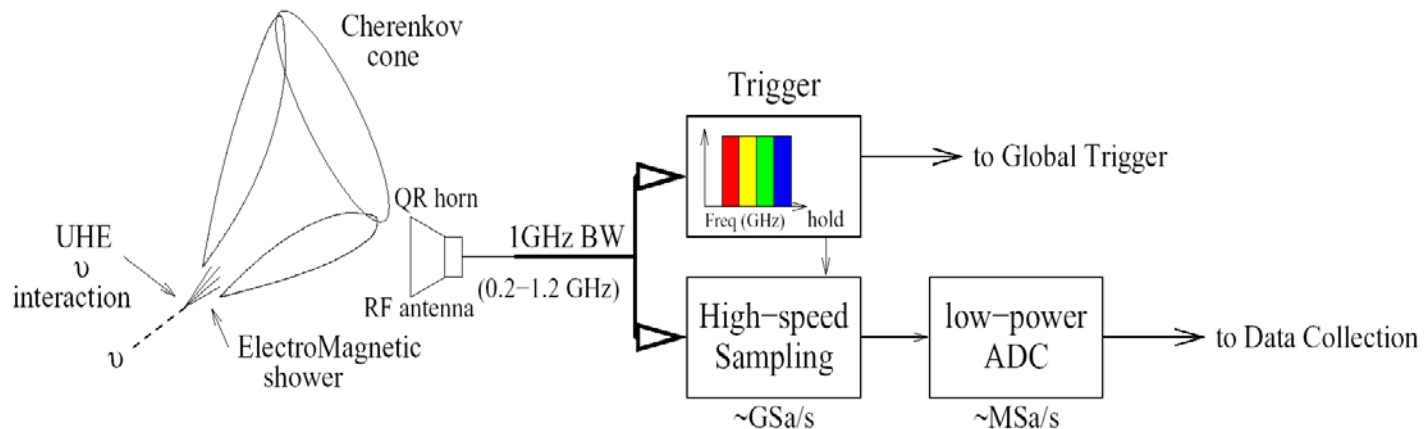
- **Excellent results obtained**
 - 1. Made the ANITA project possible & highly successful**
 - 2. Similar architectures being studied for new and upgraded experiments**
 - 3. Minimize costs for large systems**
- **Not a magic solution**
 - **Significant constraints**
 - **Technology in its infancy – will continue to improve**
- **Limits and future directions**

The technology, in a bit more detail

Constraint 0: An Intrinsic Limitation

No power (performance savings) for continuous digitization

Won't displace Flash ADCs

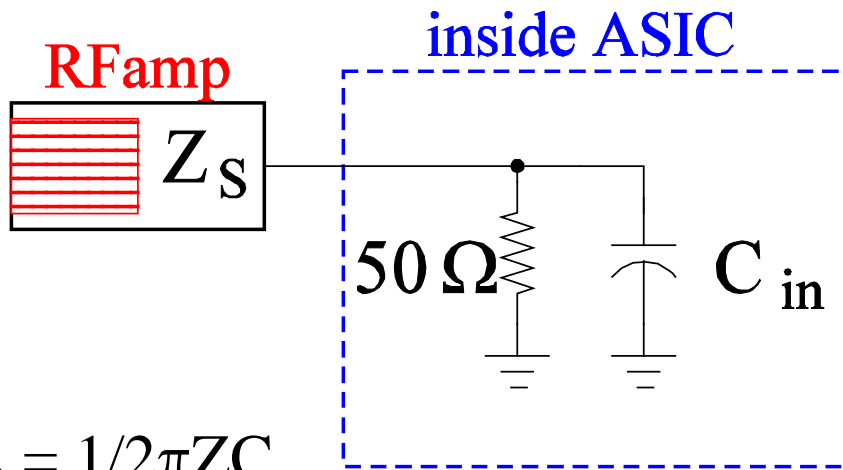


“down conversion”

→ For most “triggered” ‘event’ applications,
not a serious drawback

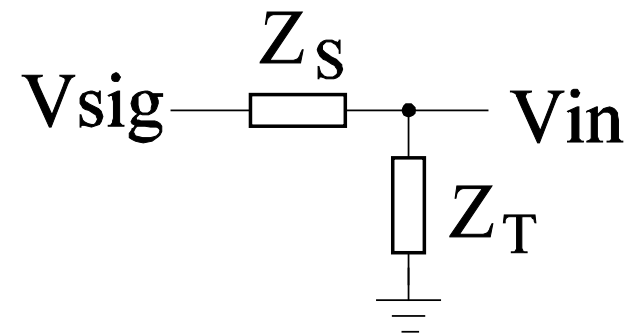
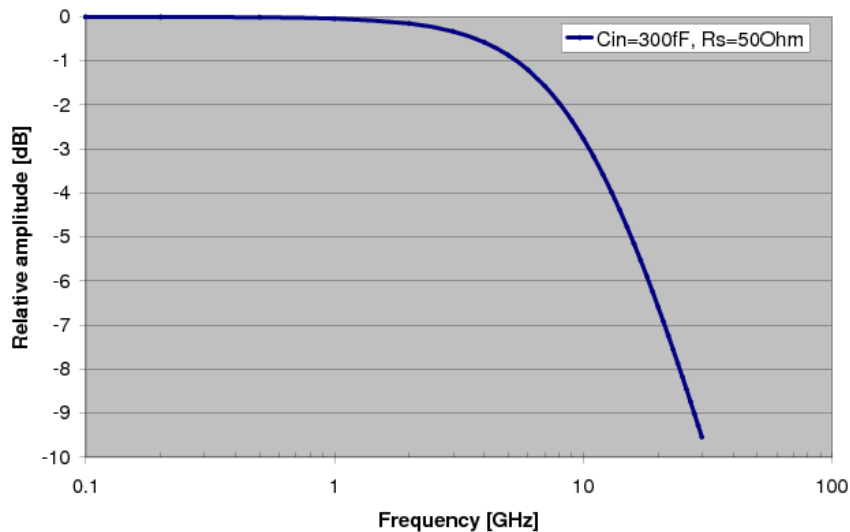
Constraint 1: Analog Bandwidth

Difficult to couple in Large BW (C is deadly)

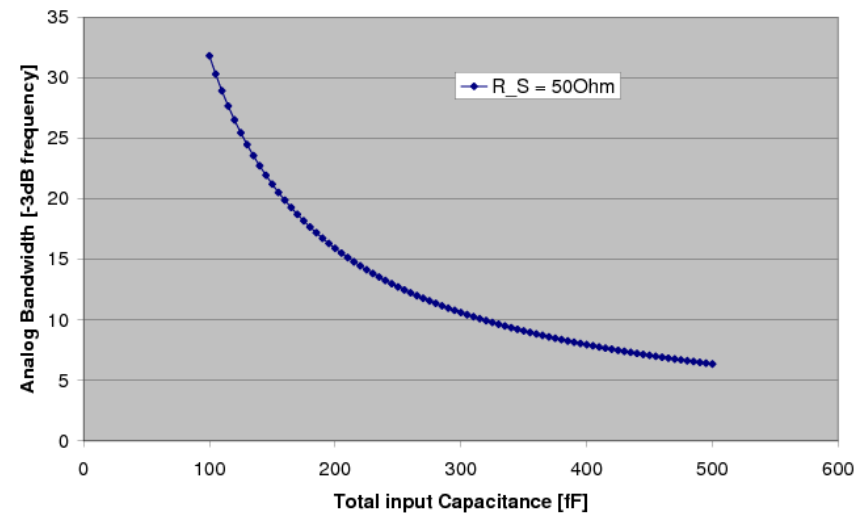


$$f_{3dB} = 1/2\pi ZC$$

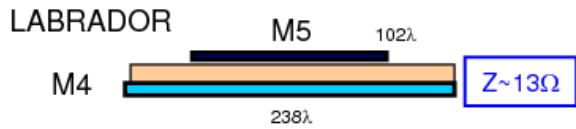
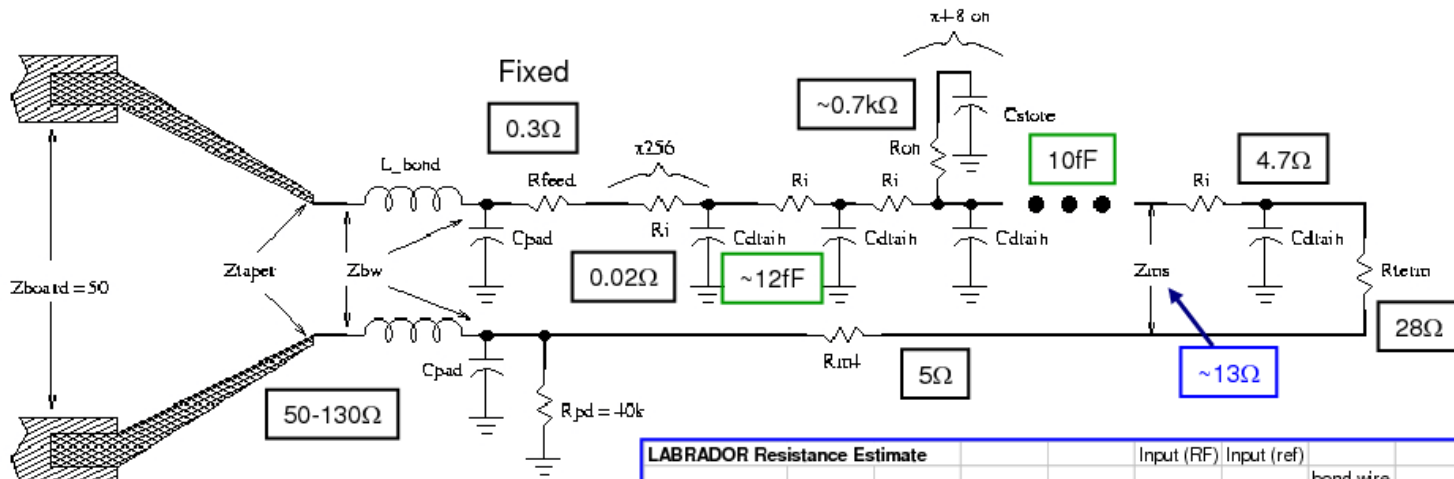
Input coupling versus frequency



Input Coupling versus total input Capacitance



Bandwidth Limitations (LAB1 example)



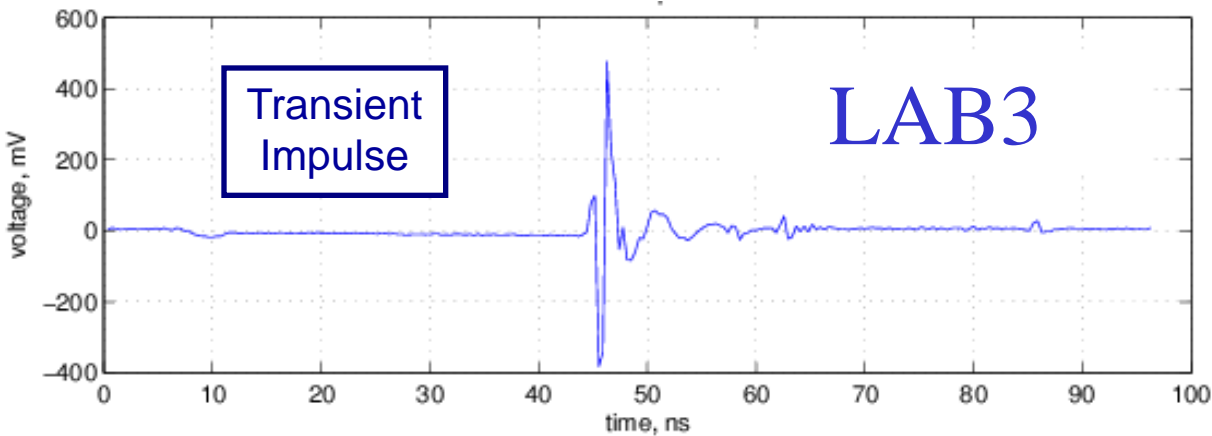
LABRADOR Resistance Estimate				Input (RF)	Input (ref)
Length	17000 λ			0.0	0.1
		70			0.2
Metal 4(sheet) =	0.07 Ohm/sq		71.42857		5.0
Metal 5(sheet) =	0.03 Ohm/sq	166.6667		5.0	5.0
Poly contact =	5.1 Ohm	6	6	0.9	0.9
via 1=	2.7 Ohm	6	3	0.5	0.9
via 2=	5.35 Ohm	6	3	0.9	1.8
via 3=	8.26 Ohm	6	3	1.4	2.8
via 4=	11.34 Ohm	6		1.9	
				10.5	11.5
					Total per feed
					28 Ωterminator
					50.0
	Measured:	Ohm			Grand Total

$$f_{3dB} = 1/2\pi ZC$$

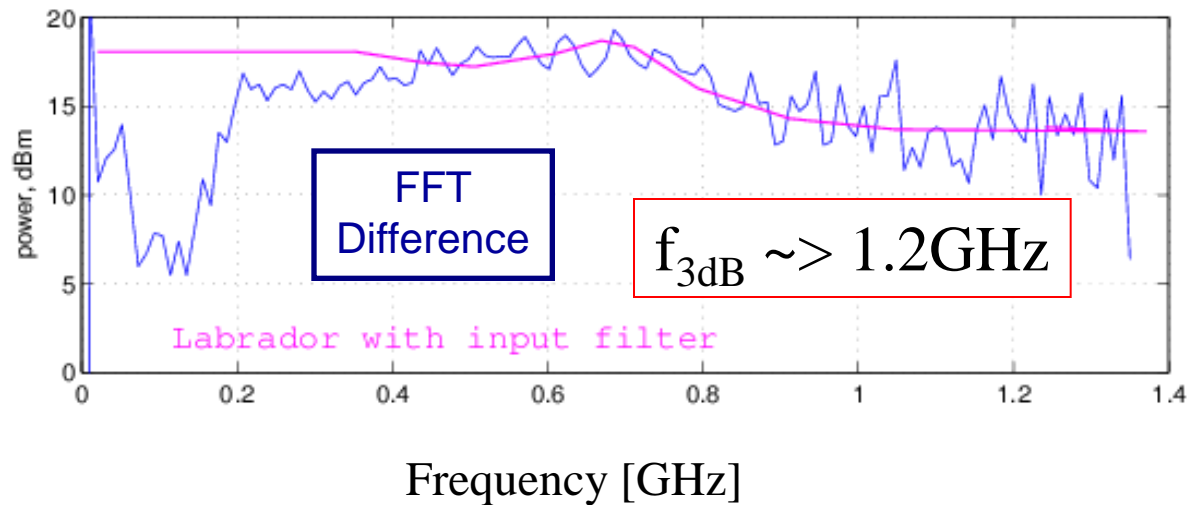
Would like smallest possible Cstore

- For 1.2GHz, $C < \sim 2\text{pF}$ (NB input protection diode $\sim 10\text{pF}$)
- Minimize C , (C_{drain} not negligible $\times 260$)

An Example Bandwidth Evaluation



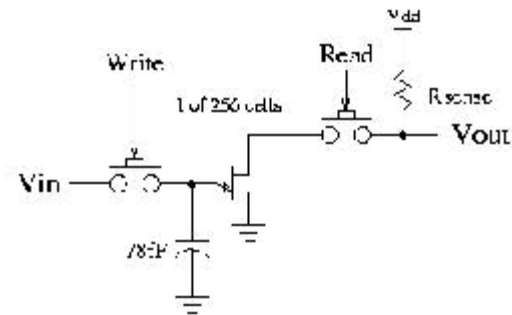
9 channels of
256 samples



To do
better,
reduce
input and
storage C

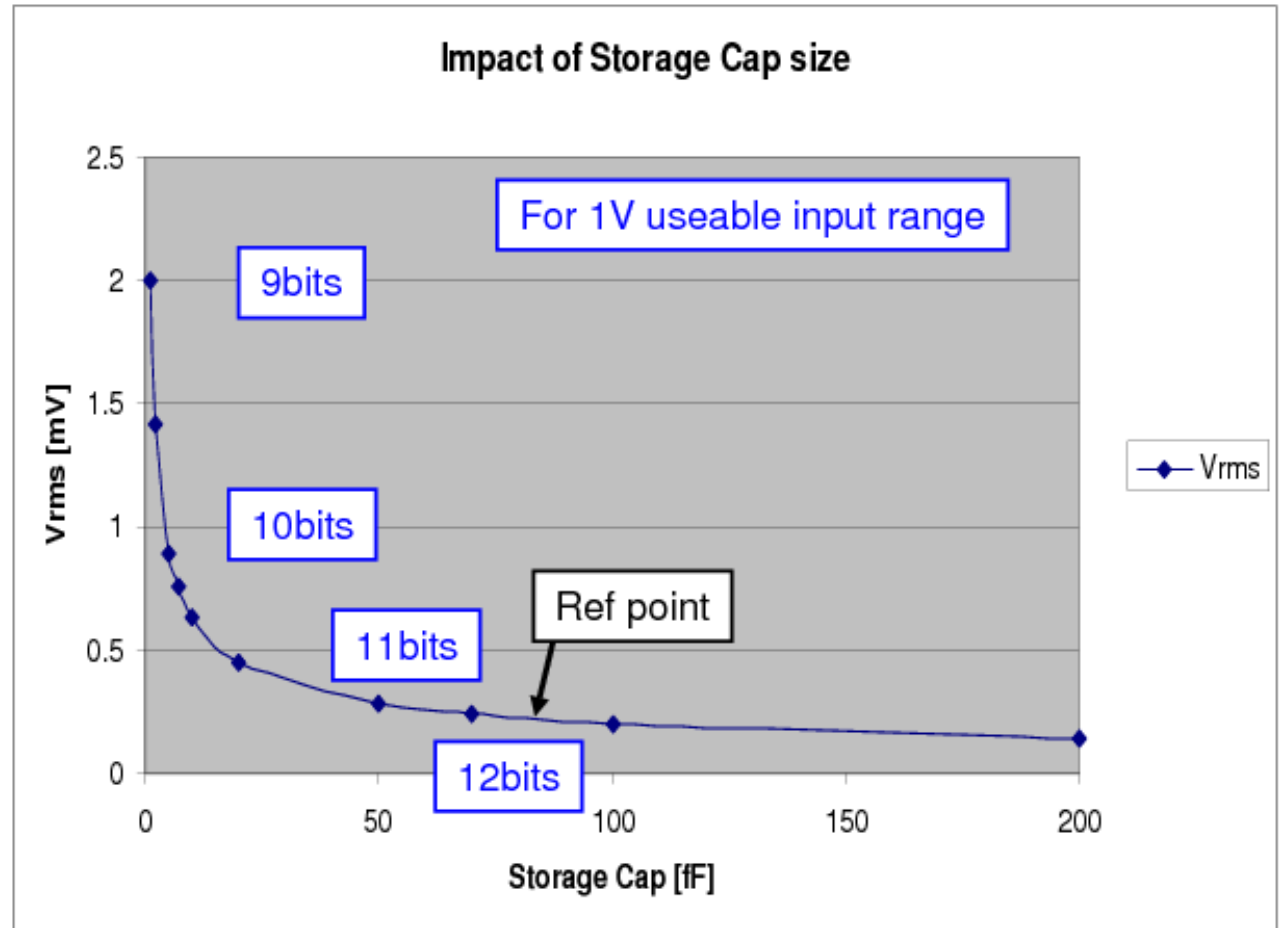
Constraint 2: kTC Noise

Want small storage C, but...



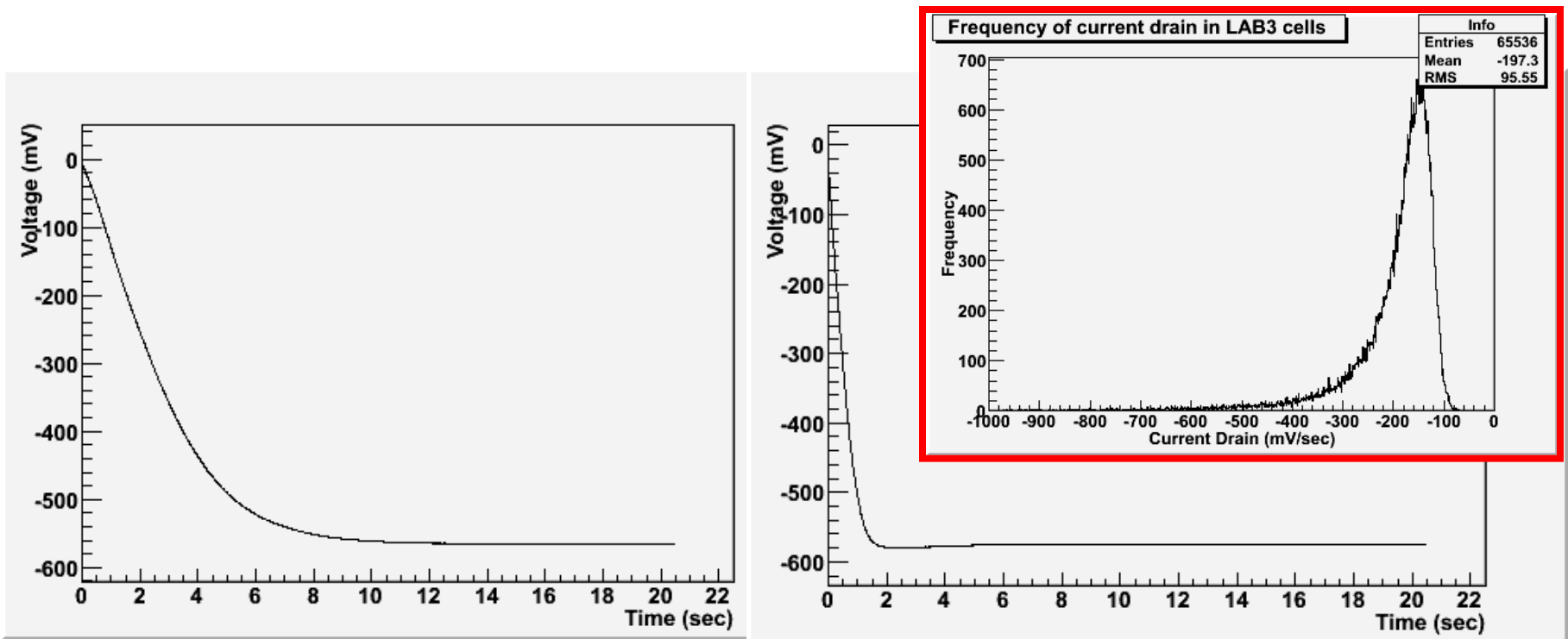
$$v_{rms} = \sqrt{\frac{kT}{C_{store}}} = 0.23mV$$

$$C_{store} = 78fF$$



Similar Constraint 2b: Leakage Current

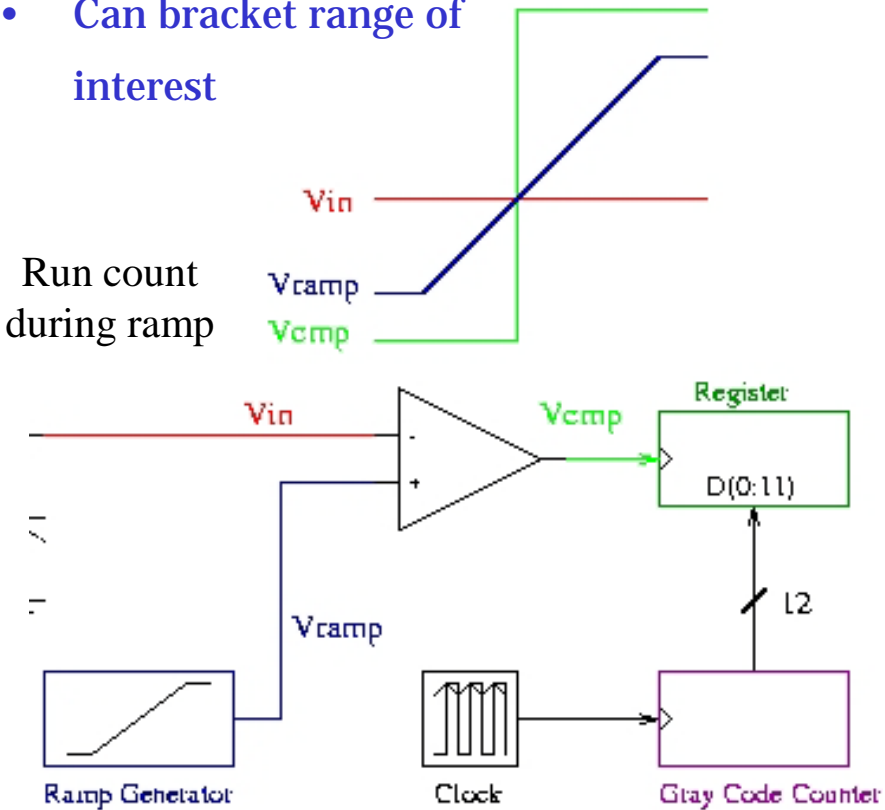
Increase C or reduce conversion time $\ll 1\text{mV}$



Sample channel-channel variation
~ fA leakage typically

Constraint 3: Digitization

- No missing codes
- Linearity as good as can make ramp
- Can bracket range of interest

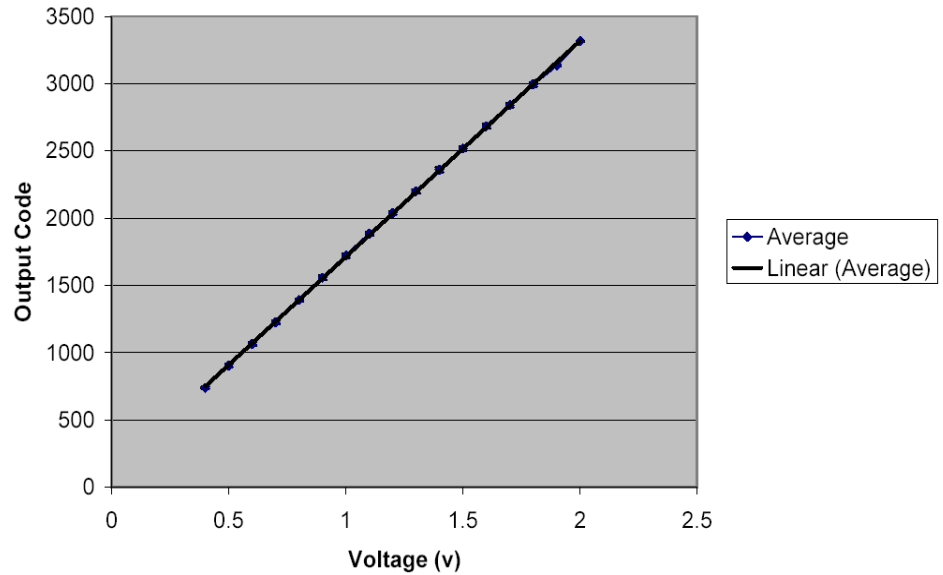


12-bit ADC

Labrador ADC Performance

$$y = 1606.8x + 105.26$$

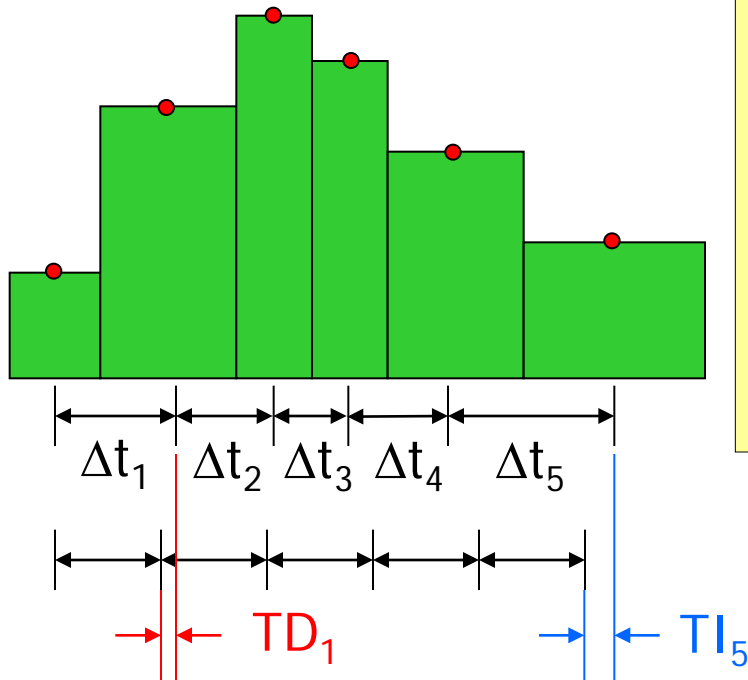
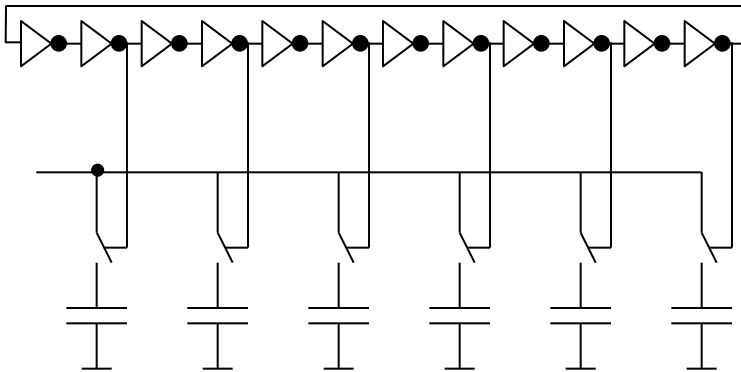
$$R^2 = 0.9999$$



Wilkinson ADC

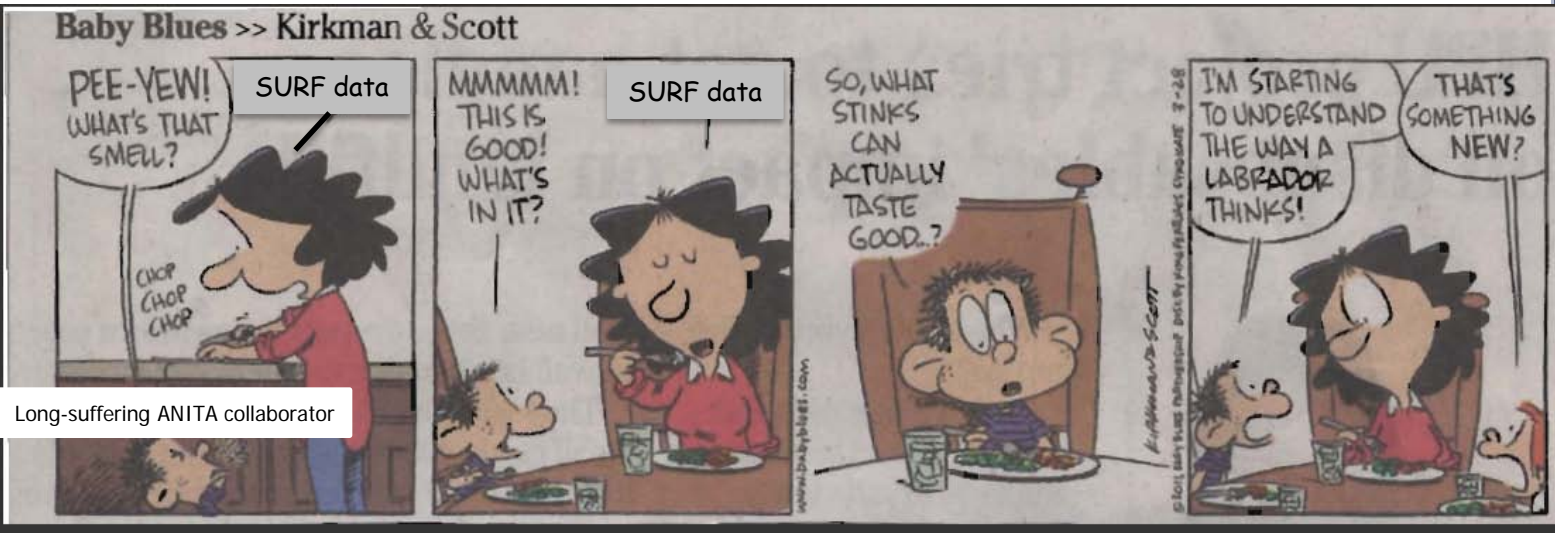
- Excellent linearity
- Basically as good as can make current source/comparator
- Comparator ~0.4 – 2.1V; 133MHz GCC max (~31us)

Constraint 4: Sample Aperture Variance



- Inverter chain has transistor variations
→ Δt_i between samples differ
→ “Fixed pattern aperture jitter”
- “Differential temporal nonlinearity”
 $TD_i = \Delta t_i - \Delta t_{\text{nominal}}$
- “Integral temporal nonlinearity”
 $TI_i = \sum \Delta t_i - i \cdot \Delta t_{\text{nominal}}$
- “Random aperture jitter” = variation of Δt_i between measurements

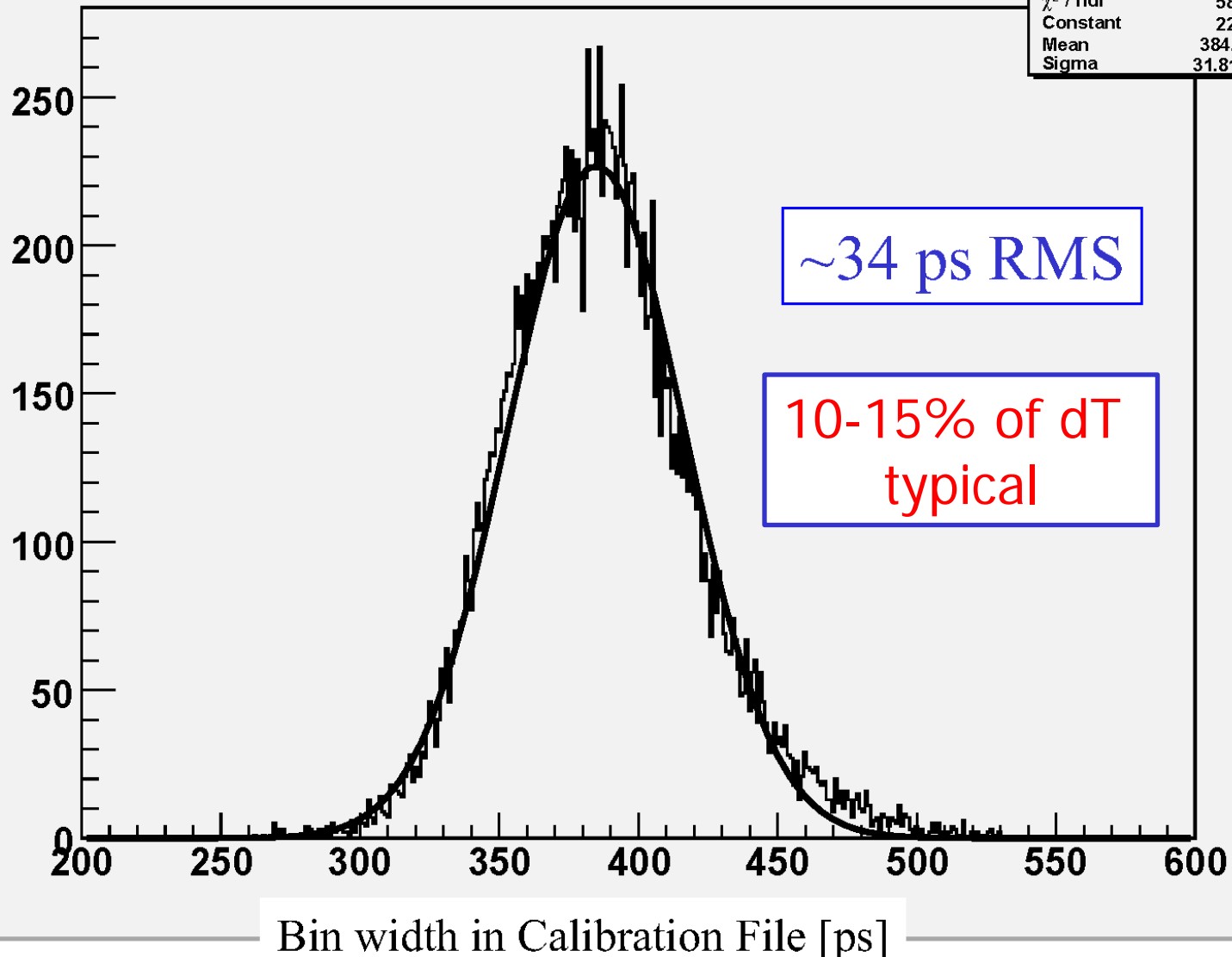
Non-uniform sampling timebase



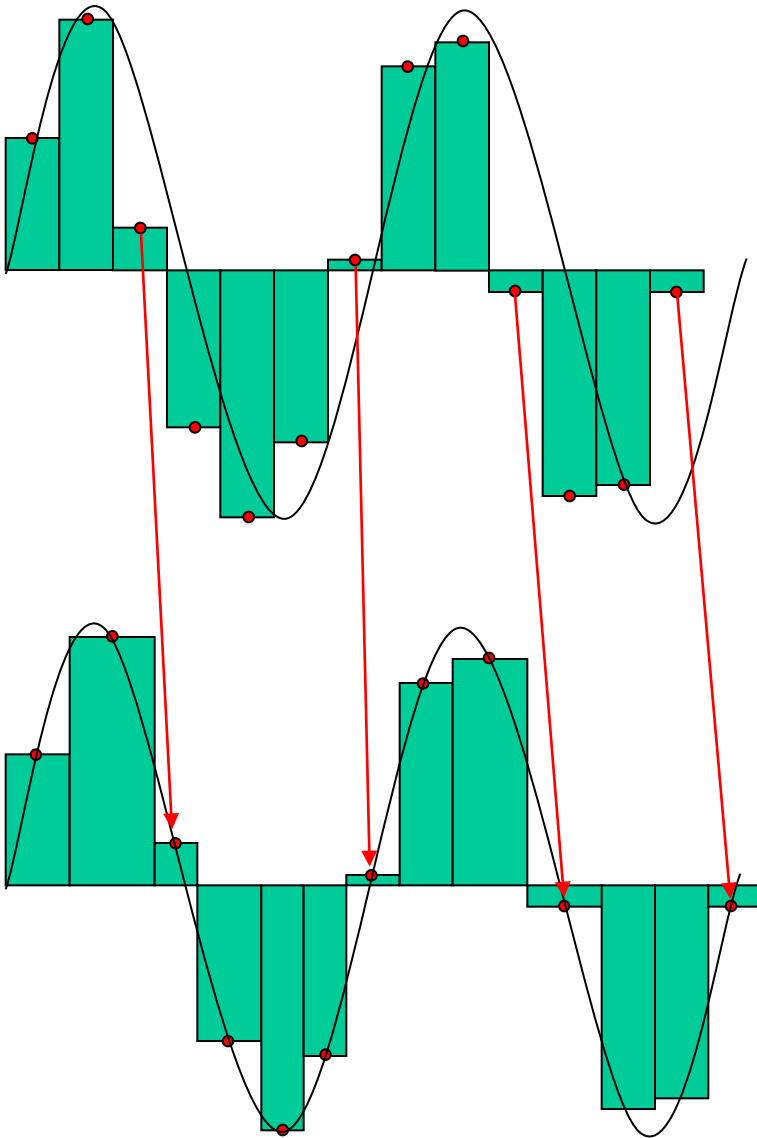
dT Spread

2.6 GSa/s [LABRADOR3]

Bin Interval	
Entries	18720
Mean	386
RMS	34.3
χ^2 / ndf	582 / 253
Constant	227 ± 2.2
Mean	384.8 ± 0.2
Sigma	31.81 ± 0.19

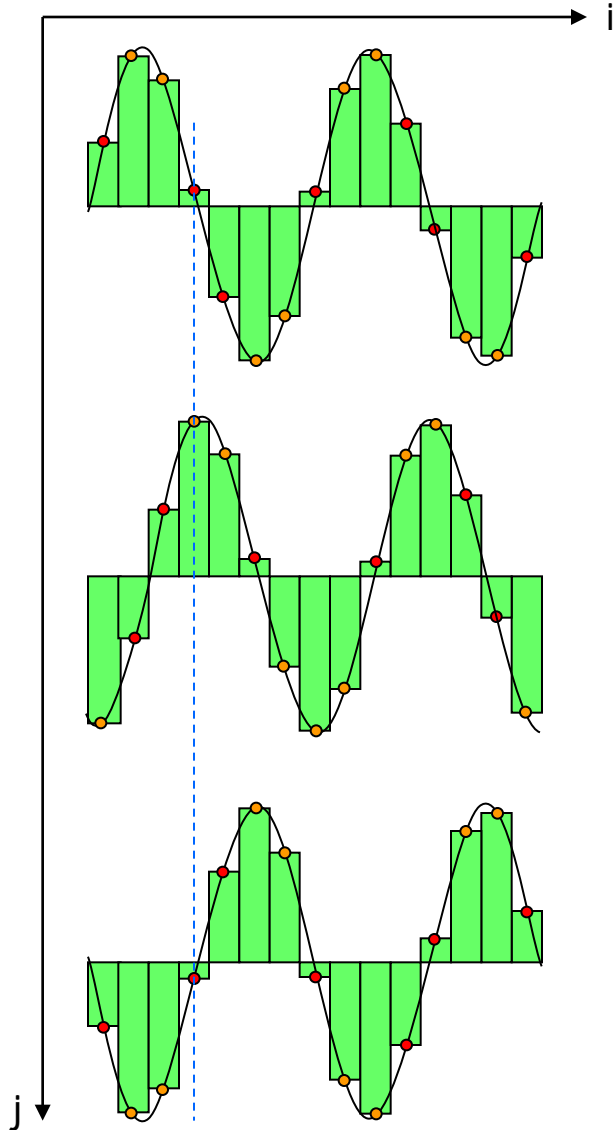


Average aperture calibration



- Fixed aperture offsets are constant over time, can be measured and corrected
- Several methods are commonly used (sine fit [left], zero-crossing)
- Most use sine wave with random phase and correct for TD_i on a statistical basis

Sine Curve Fit Method



$$\chi^2 = \sum_{j=0}^{500} \sum_{i=0}^{1024} (y_{ji} - (a_j \sin(i \frac{2\pi}{f_j} + \alpha_j + \beta_i) + o_j))^2 \rightarrow \min$$

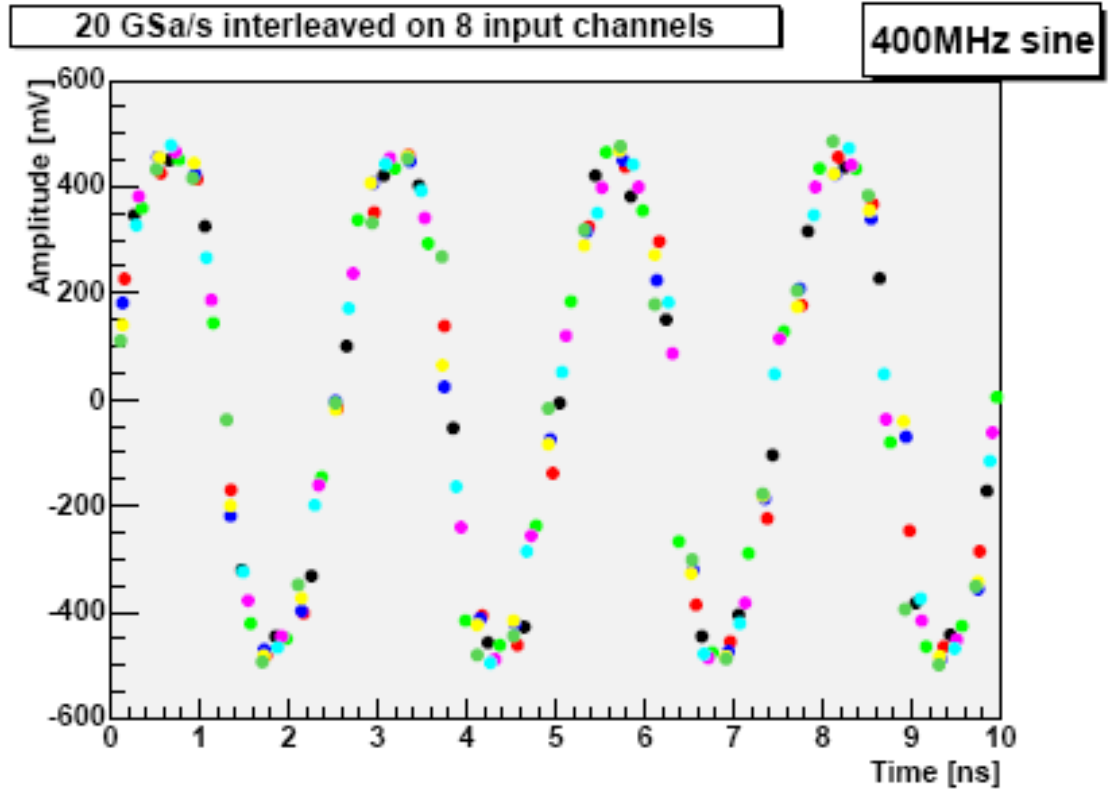
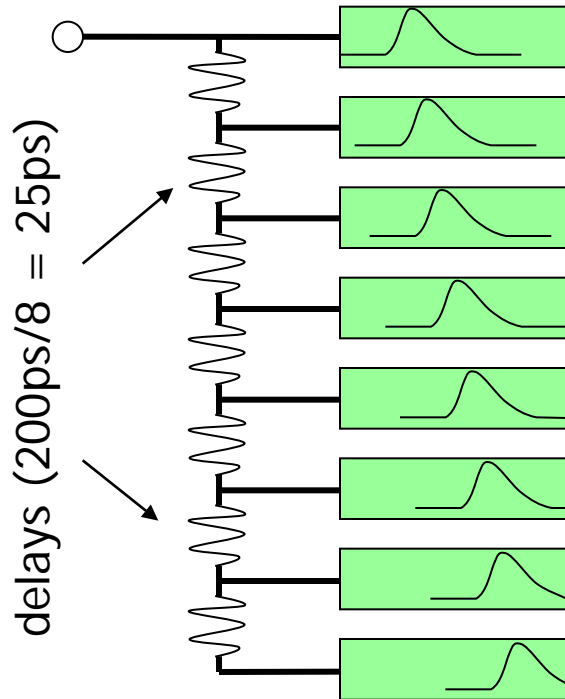
y_{ji} : i-th sample of measurement j
 $a_j f_j \alpha_j o_j$: sine wave parameters
 β_i : phase error \rightarrow fixed jitter

“Iterative global fit”:

- Determine rough sine wave parameters for each measurement by fit
- Determine β_i using all measurements where sample “i” is near zero crossing
- Make several iterations

Option 1: Even Faster Sampling

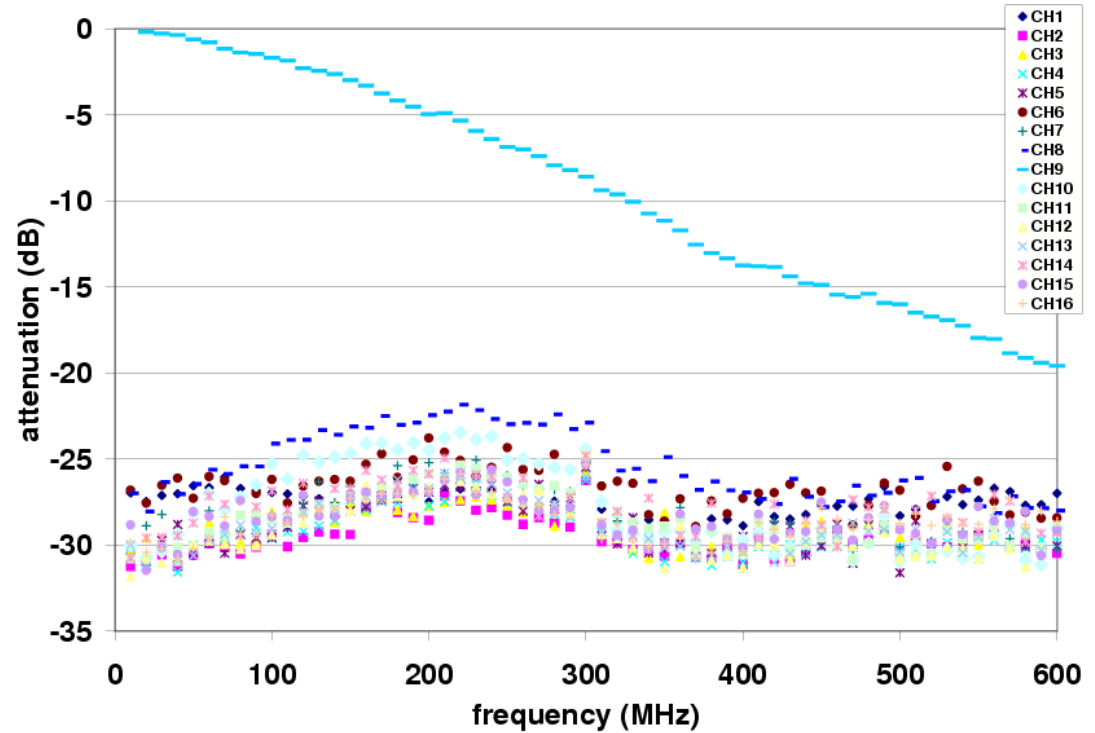
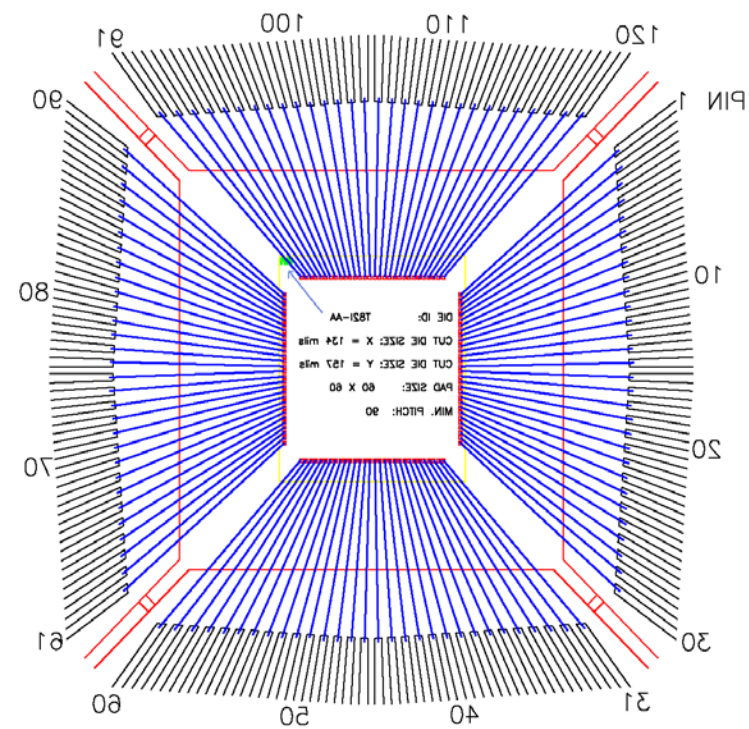
6 GSPS * 8 = 48 GSPS



Possible with delay is implemented on PCB

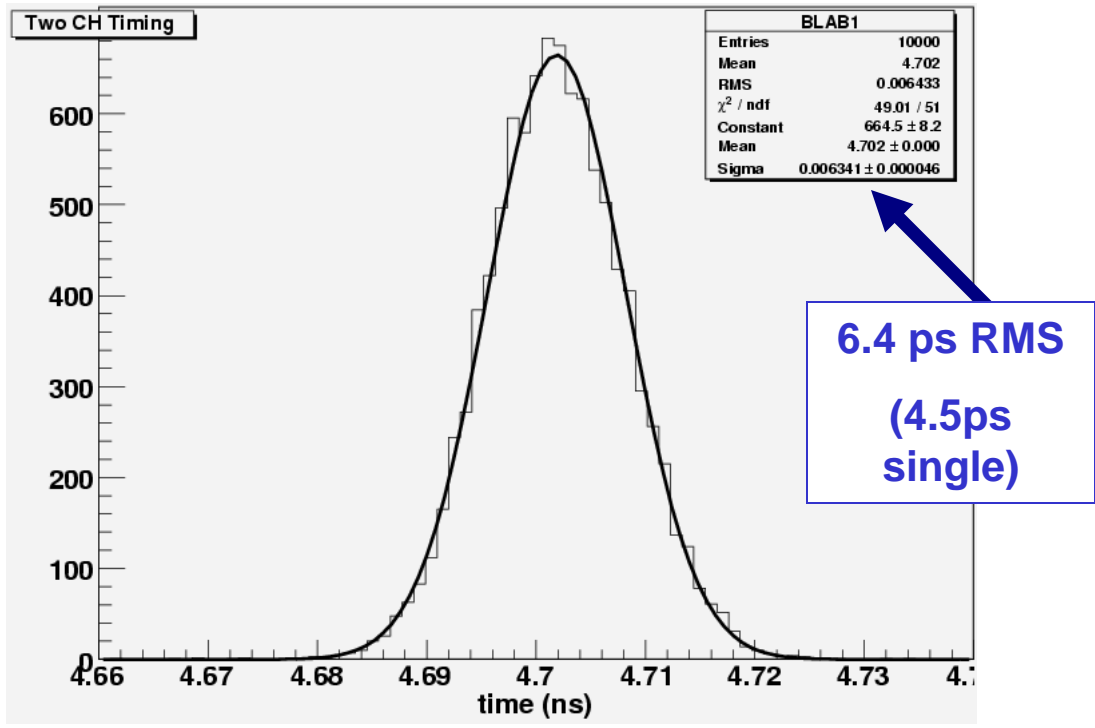
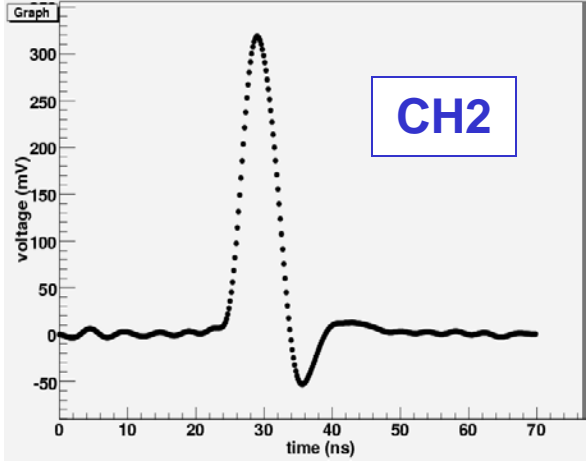
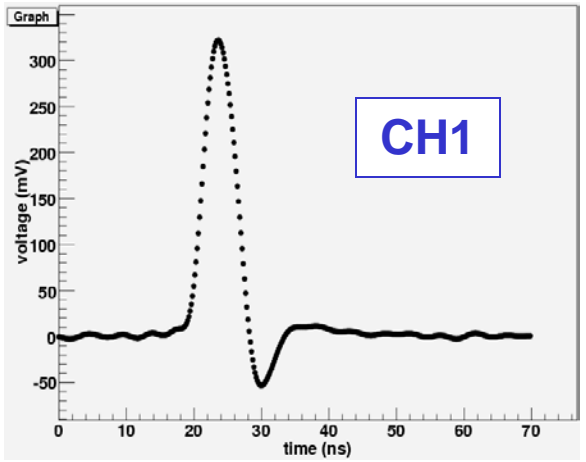
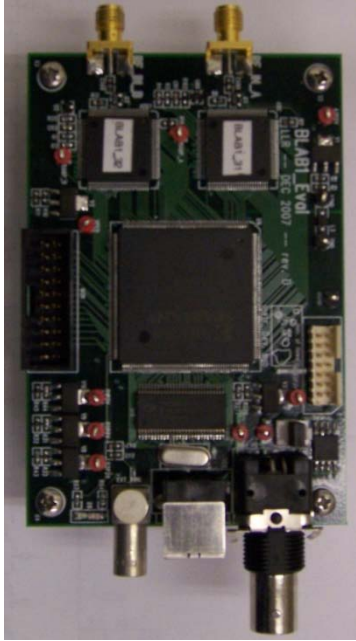
Constraint 5: Cross-talk

Coupling between wire-bonds, V_{ref}



Advantage 1: Compact, low-power

- Comparable performance to best CFD + HPTDC
- Time difference measurement of recorded pulses
- Using full samples significantly reduces the impact of noise

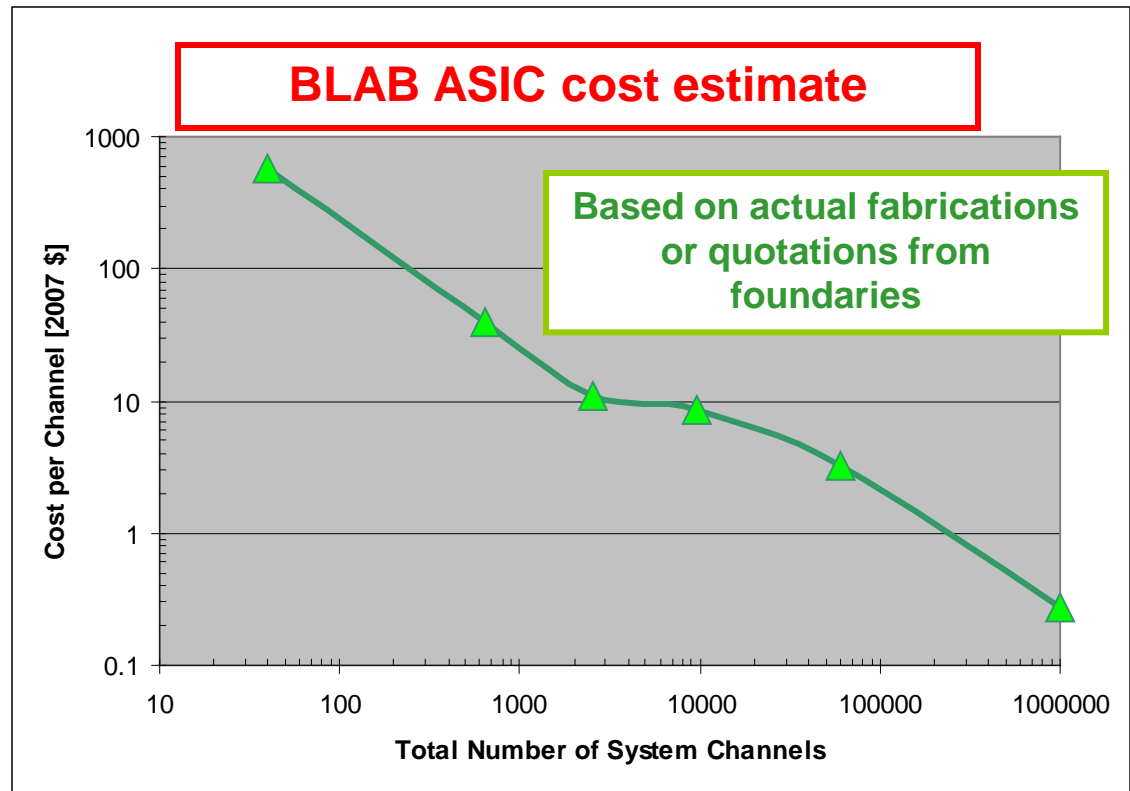
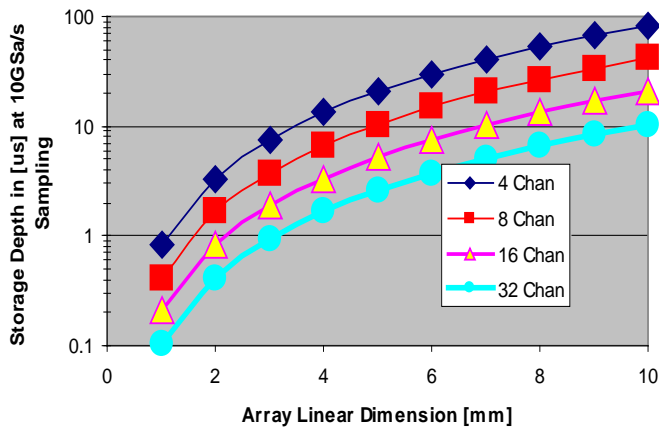


Advantage 2: Scaling to Large Systems

- ASIC costing well understood, very competitive!

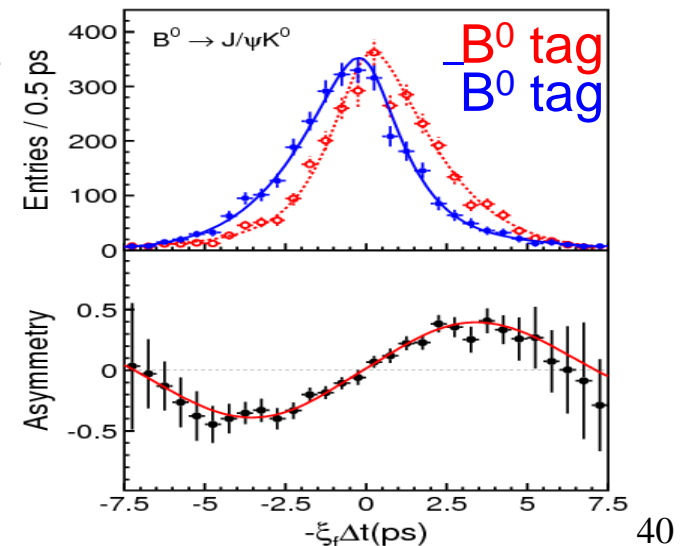
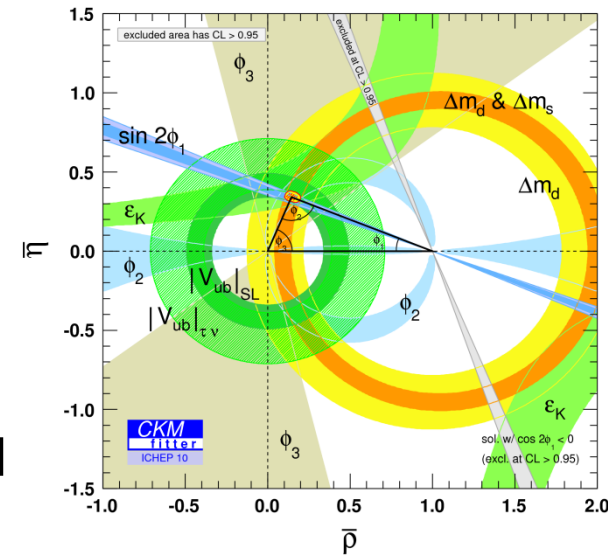
NIM A591 (2008) 534-345.

Storage Depth Capacity



B-factory Detectors – a huge success!

- Measurements of CKM matrix elements and angles of the unitarity triangle
- Observation of direct CP violation in B decays
- Measurements of rare decays (e.g., $B \rightarrow \tau \nu$, $D \tau \nu$)
- $b \rightarrow s$ transitions: probe for new sources of CPV and constraints from the $b \rightarrow s \gamma$ branching fraction
- Forward-backward asymmetry (A_{FB}) in $b \rightarrow s ll$ has become a powerful tool to search for physics beyond SM.
- Observation of D mixing
- Searches for rare τ decays
- Observation of new hadrons



Are we done yet ?



BAU: CKM
mechanism still
short by 10 orders of
magnitude.

Из эссе С. Окубо
при большой температуре
для Вселенной смена знака
но ее кривой фигуре

НАРУШЕНИЕ CP-ИНВАРИАНТНОСТИ, C-АСИММЕТРИЯ
И БАРИОННАЯ АСИММЕТРИЯ ВСЕЛЕННОЙ

А.Д.Сазаров

Теория расширяющейся Вселенной, предполагающая сверхплотное начальное состояние вещества, по-видимому, исключает возможность макроскопического разделения вещества и антивещества; поэтому следует



“Super” B Factory strategy

B factories → **is SM with CKM right?**

Super B factories → **How is the SM wrong?**

→ **Need much more data (two orders!)** because the SM worked so well until now → **Super B factory**

However: it will be a **different world** in four years, there will be serious competition from **LHCb** and **BESIII** → **PANDA**

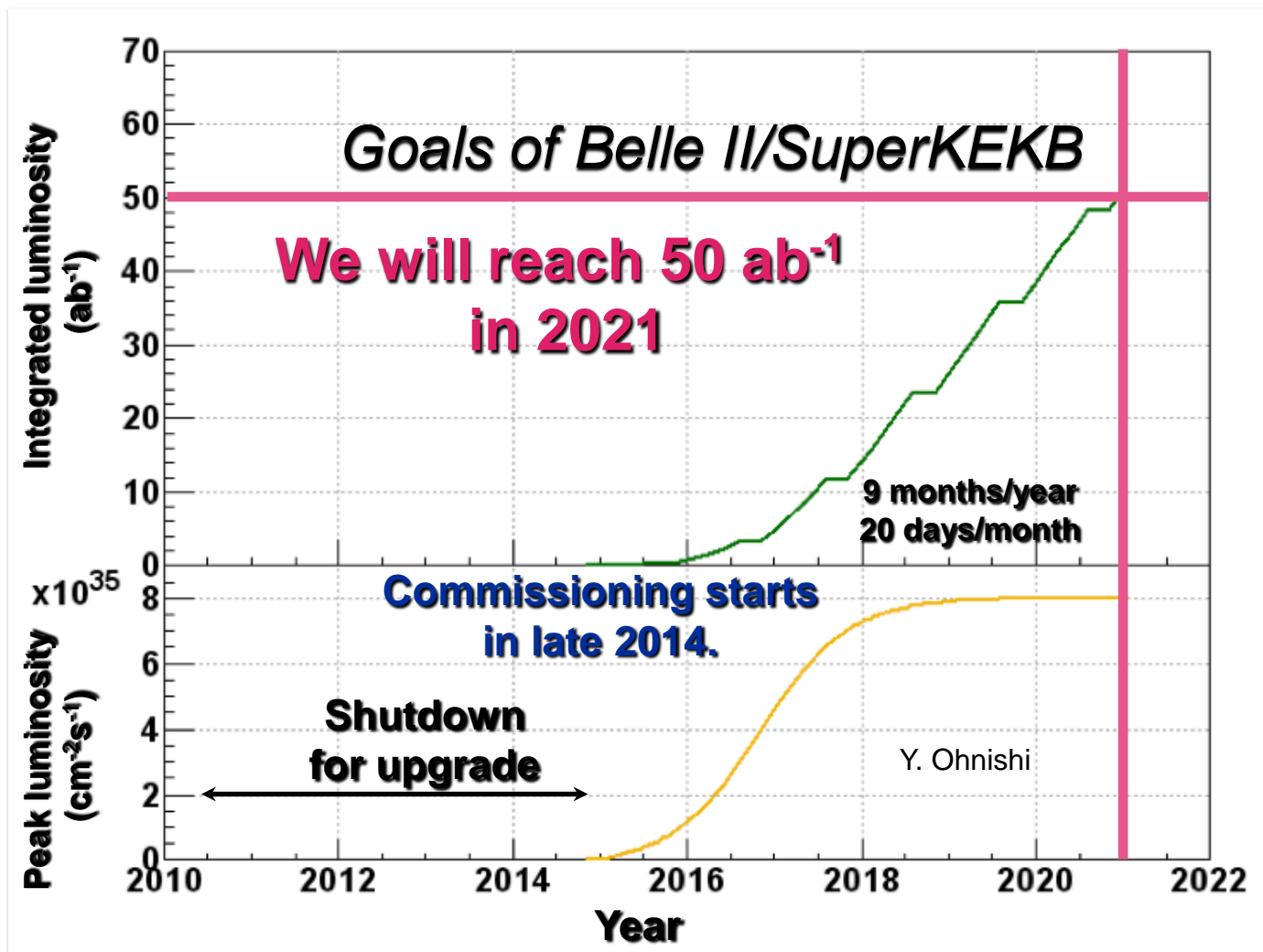
Still, e^+e^- machines running at (or near) $\Upsilon(4s)$ will have **considerable advantages in several classes of measurements**, and will be **complementary in many more**

Update of the physics reach with 50 ab^{-1} (75 ab^{-1}):

Physics at Super B Factory (Belle II authors + guests) [hep-ex](#) > arXiv:1002.5012

SuperB Progress Reports: Physics (SuperB authors + guests) [hep-ex](#) > arXiv:1008.1541

SuperKEKB luminosity profile



Requirements for the Belle II detector

Critical issues at $L = 8 \times 10^{35}/\text{cm}^2/\text{sec}$

► Higher background ($\times 10\text{-}20$)

- radiation damage and occupancy
- fake hits and pile-up noise in the EM Calorimeter

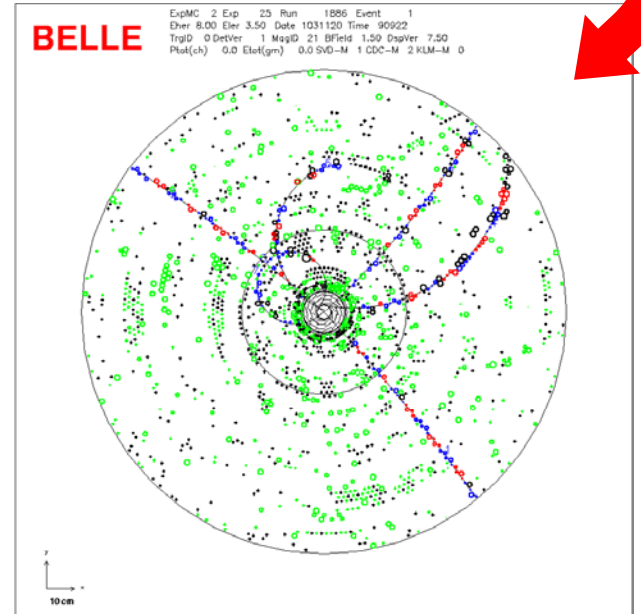
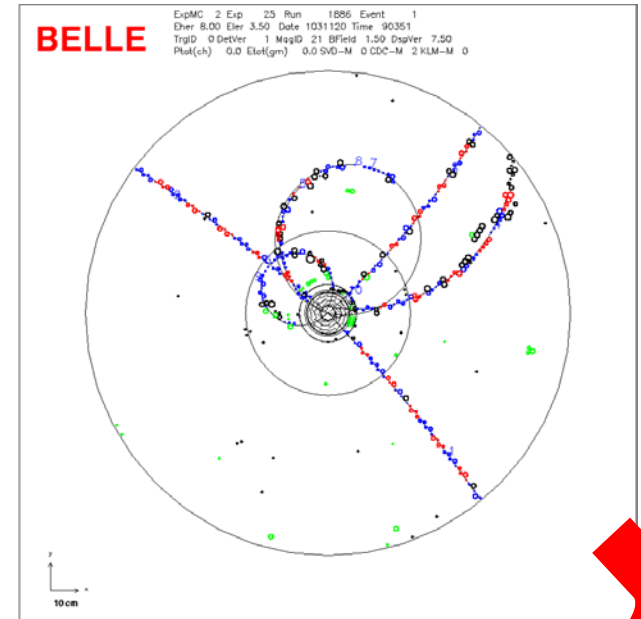
► Higher event rate ($\times 10$)

- higher rate trigger, DAQ and computing

► Special features required

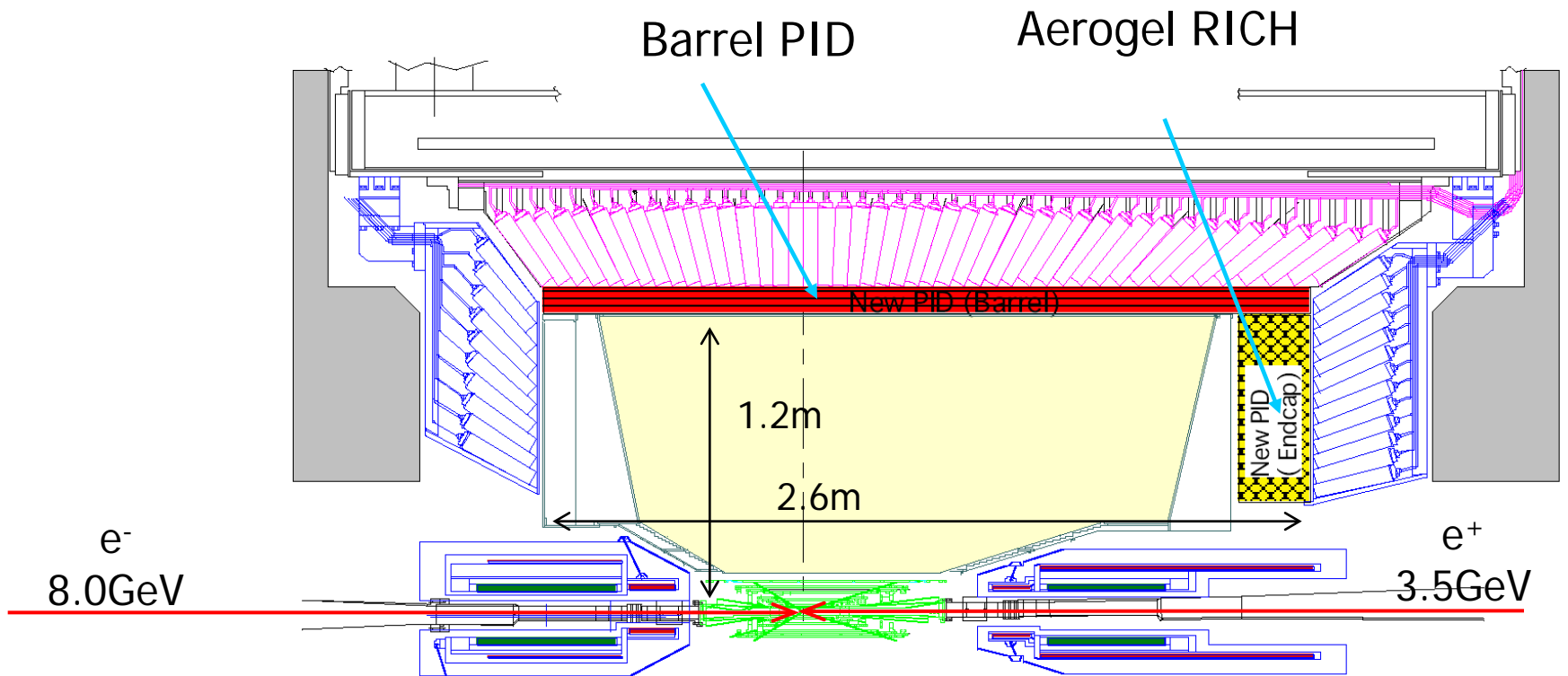
- low $p \mu$ identification $\leftarrow \sigma_{\mu\mu}$ recon. eff.
- hermeticity $\leftarrow \nu$ "reconstruction"

Result: significant upgrade



Upgraded Belle detector

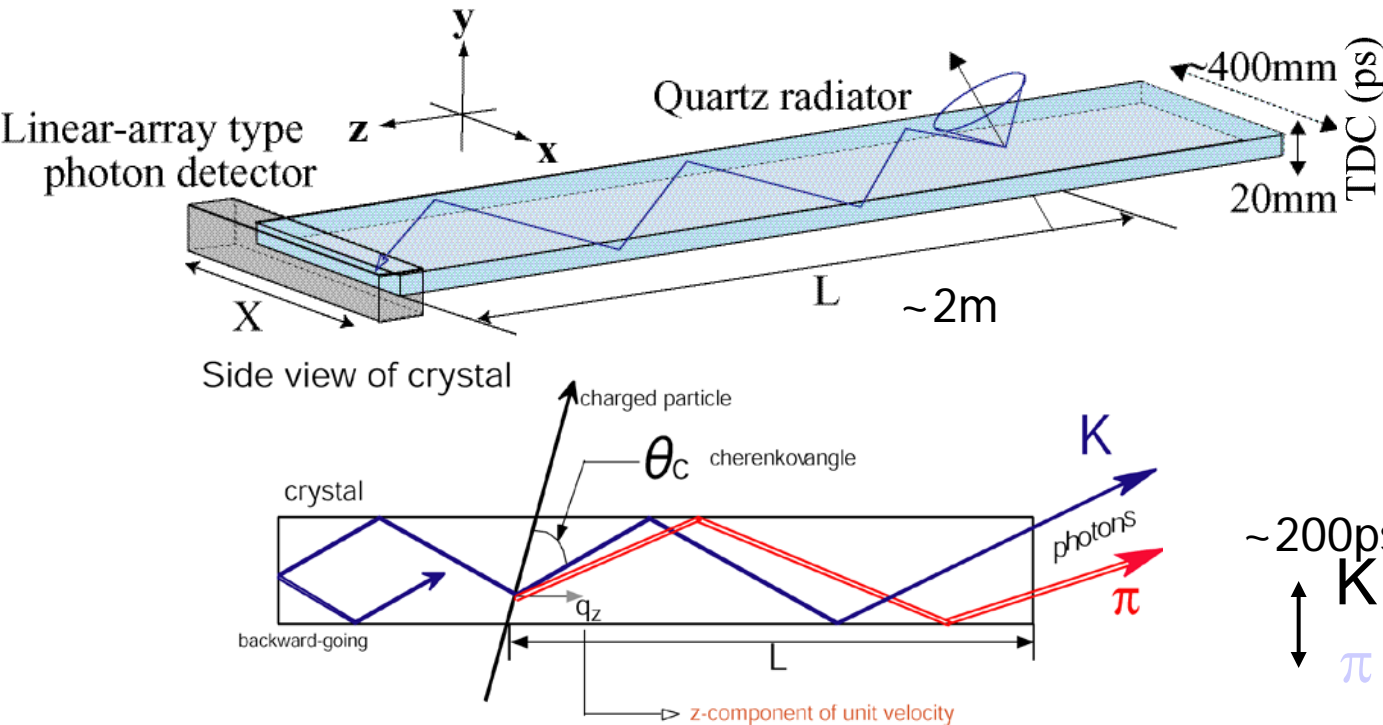
- PID (π/K) detectors
- Inside current calorimeter
- Use less material and allow more tracking volume
→ Available geometry defines form factor



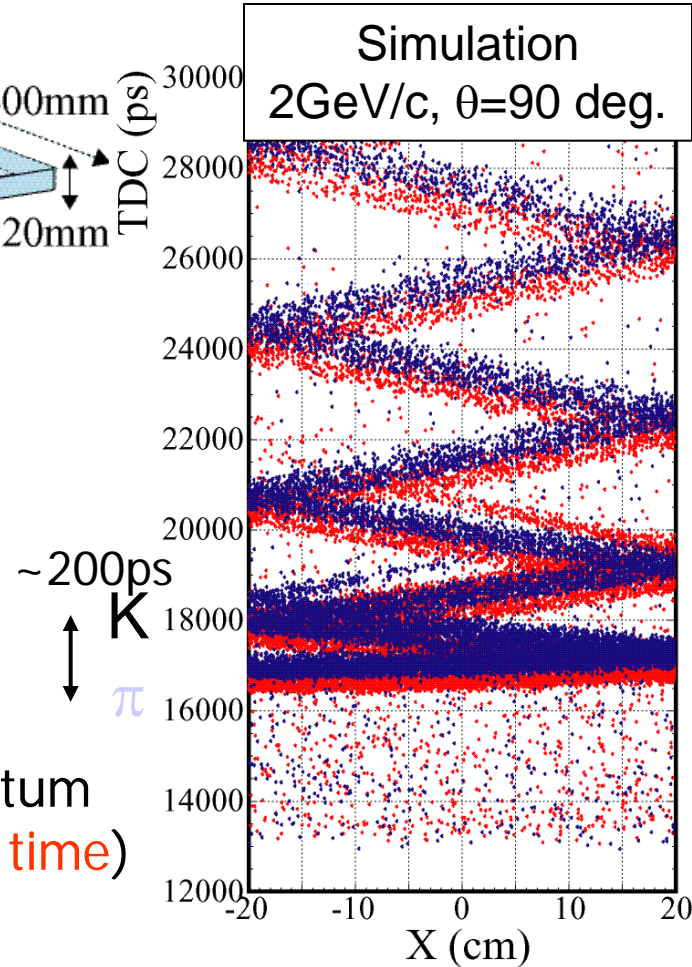
Original TOP counter concept

Linear array PMT (~5mm)
Time resolution $\sigma \sim 40\text{ps}$

- Measure Position+Time

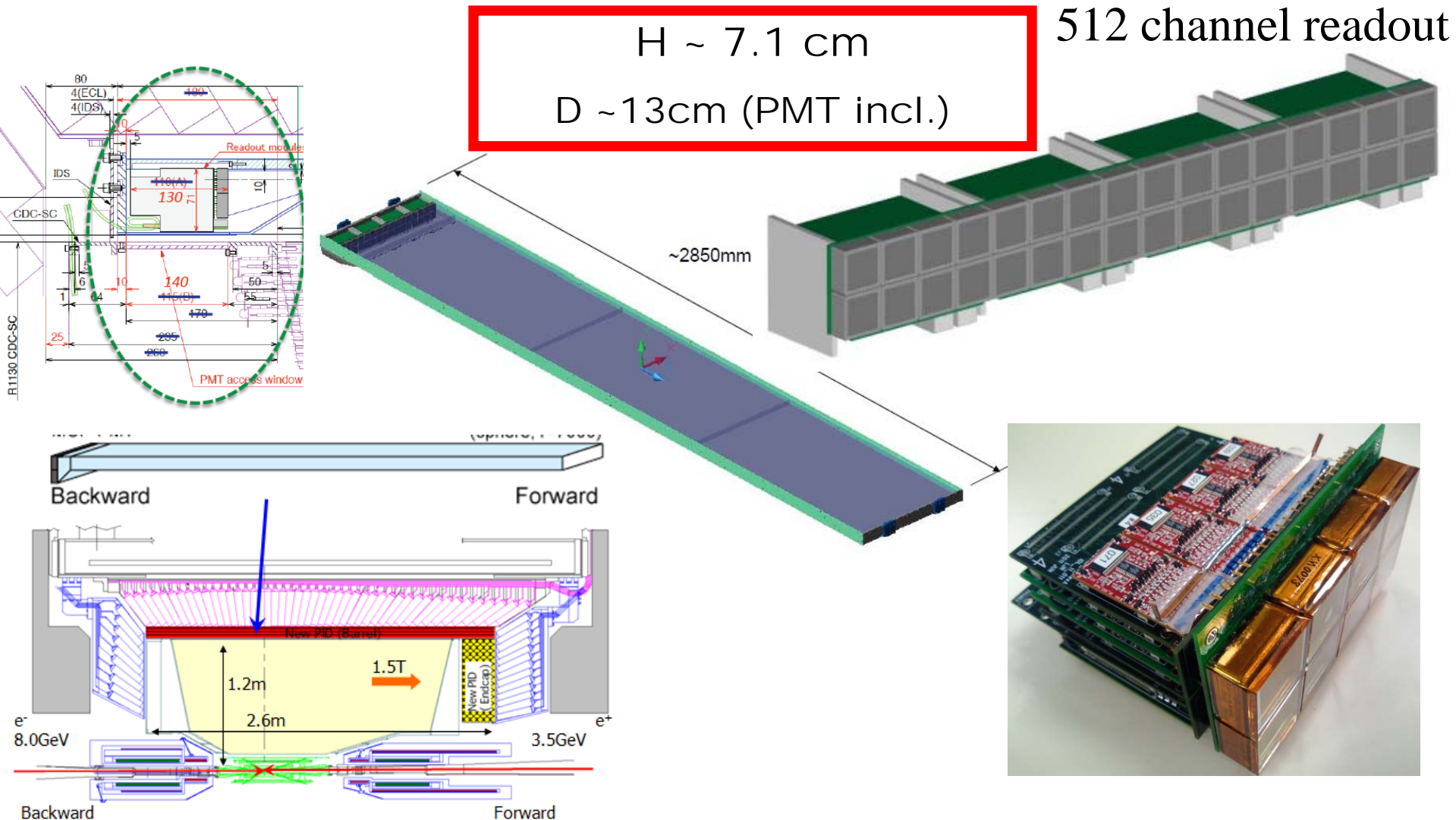


Different opening angle for the same momentum
 \rightarrow Different propagation length(= **propagation time**)
 + **TOF from IP** works additively.



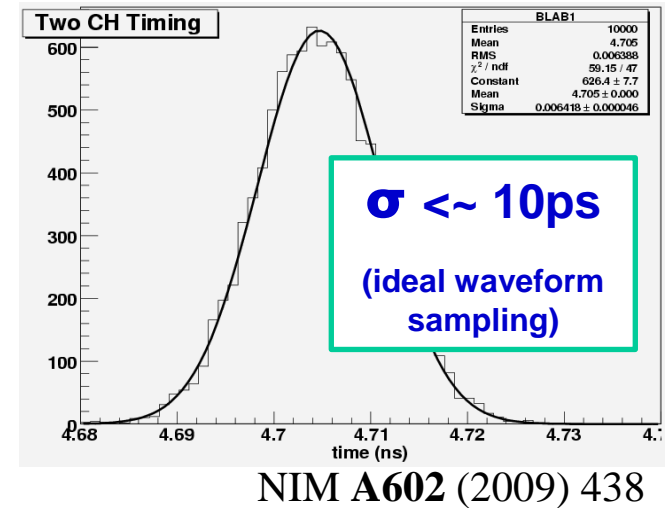
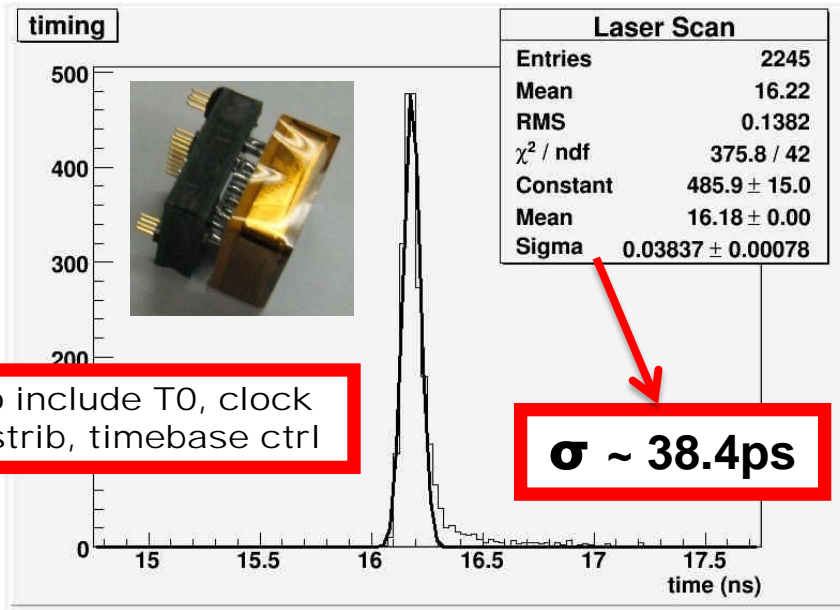
Slightly Enhanced "image plane"

- Must fit in a very crowded envelope

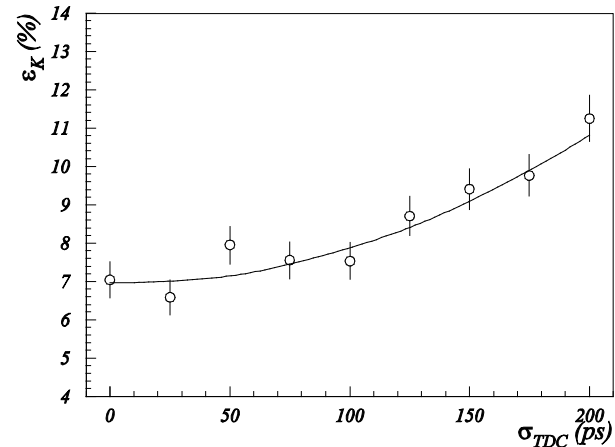
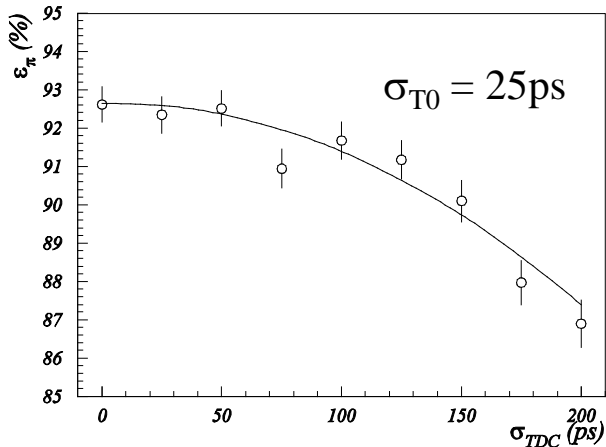


Performance Requirements (TOP)

- Single photon timing for MCP-PMTs



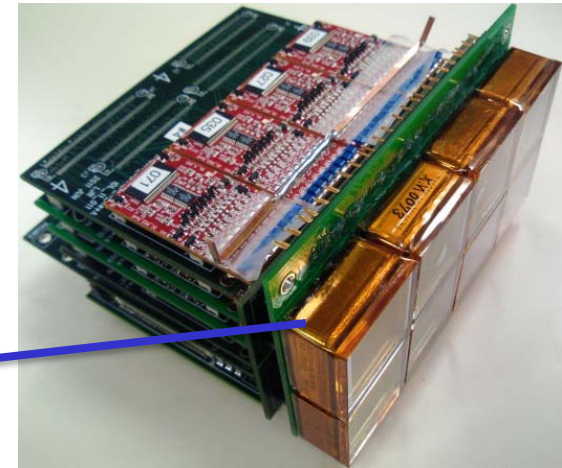
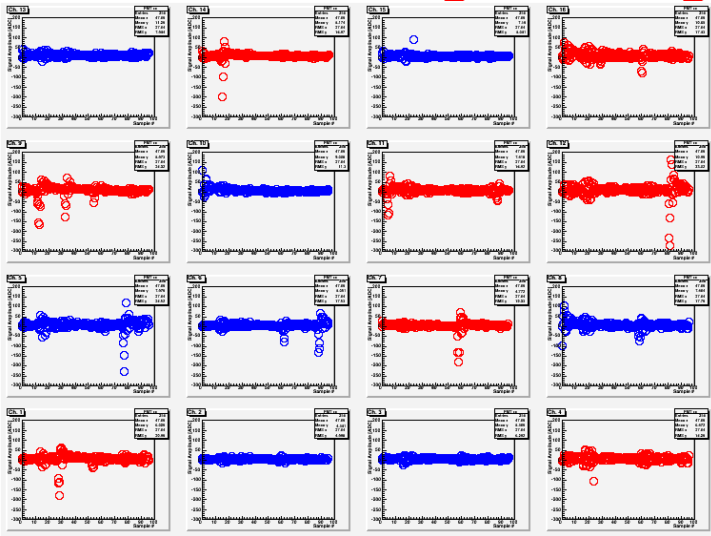
$\sigma < \sim 50\text{ps}$ target



NOTE: this is single-photon timing, not event start-time “T₀”

Readout Option Chosen

- Why Waveform Sampling?
- Lower power, high density, cost effective
- Handle charge-sharing/cross-talk



Single PMT (beam test data – 90ns windows)

Leverage experience from radio-neutrino work (≤ 30 ps on large, solar-powered payload)

- Why Not use existing ASIC?
- No suitable existing ASICs (reason why current ASICs developed)
- BLAB/IRS are only GSa/s SCA ASICs with $5\mu\text{s}$ depth (L1 trig)
- Triggerless operation? \rightarrow higher power, 330x data rate

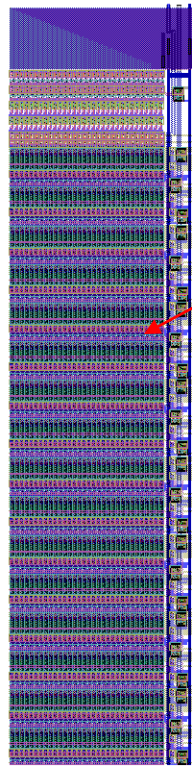
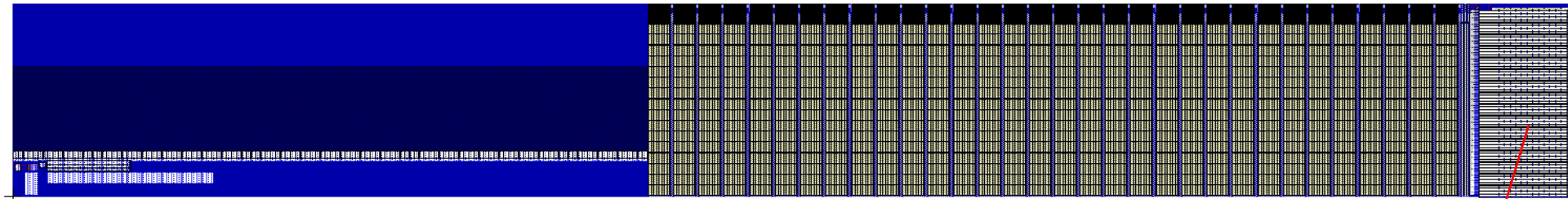
Readout ASIC Specifications

32768	samples/chan (>5.2 μ s trig latency)
8	channels/BLAB3 ASIC
8	Trigger channels
~9	bits resolution (12[10]-bits logging)
64	samples convert window (~16ns)
4	GSa/s
1	word (RAM) chan, sample readout
1+n*0.02	μ s to read n samples (of same 64)
30	kHz sustained readout (multibuffer)

- **Time alignment critical**
 - Synchronize sampling to accelerator RF clock (Belle TOF)
 - >5 μ s buffer depth a must for trigger, since single photon rates high

ASIC Single Channel

- Sampling: 128 (2x 64) separate transfer lanes
- Recording in one set 64, transferring other (“ping-pong”)

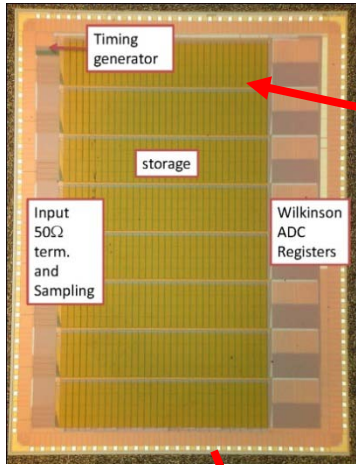


- Concurrent Writing/Reading
- Only 128 timing constants
- Storage: 64 x 512 (512 = 8 * 64)
- Wilkinson (64x1): was (32x2)
 - 64 conv/channel

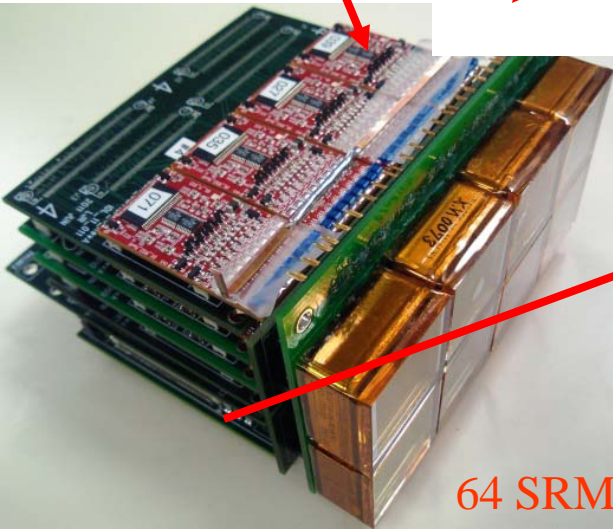
TOP Readout Architecture

16 COPPER

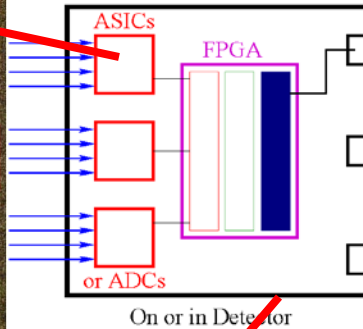
Waveform sampling ASIC



8k channels
1k 8-ch. ASICs



Subdetector Readout Module

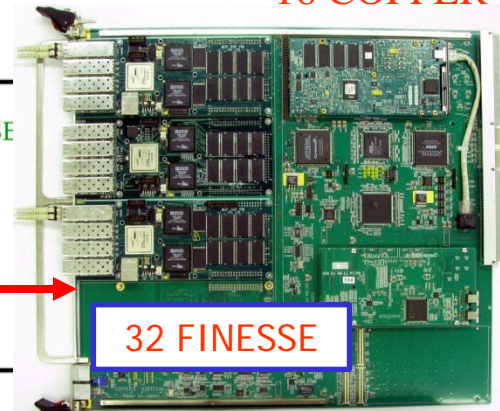
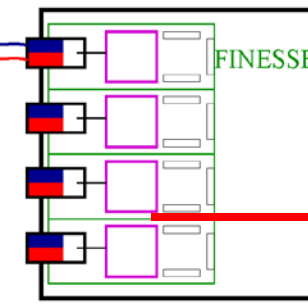


FPGA firmware consists of 3 parts:

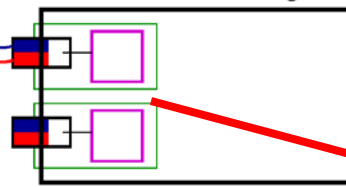
- 1) ASIC/ADC driver (common)
- 2) Trigger feature extract (subdet. specific)
- 3) Unified DAQ transport protocol

Giga-bit Fiber Transceiver Links

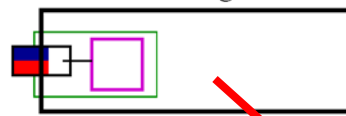
COPPER



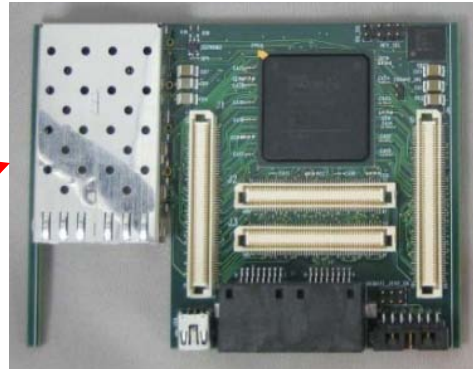
Global Decision Logic



Clock/Event Timing Distribution



Clock jitter cleaners



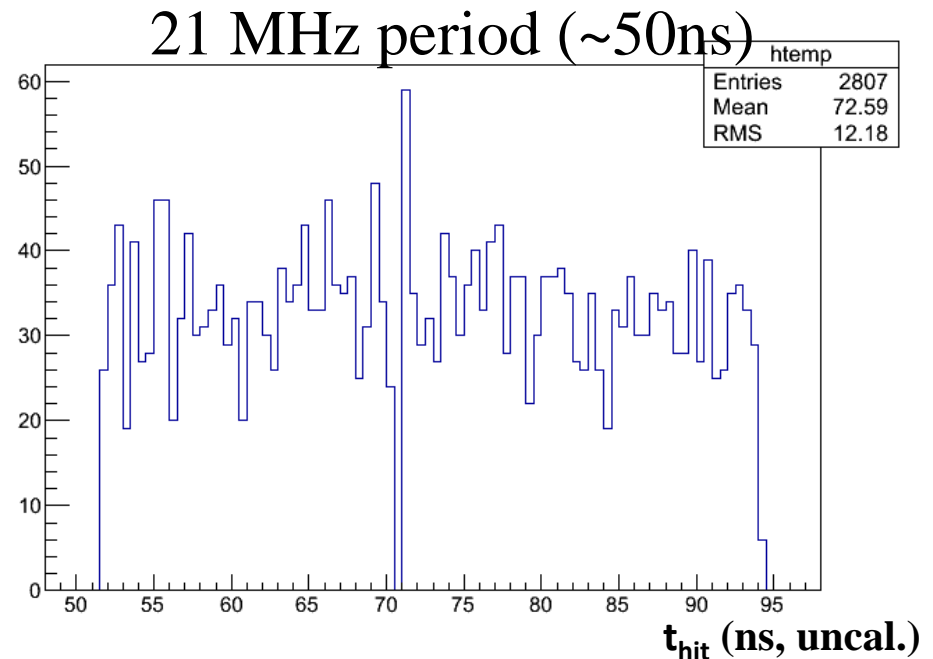
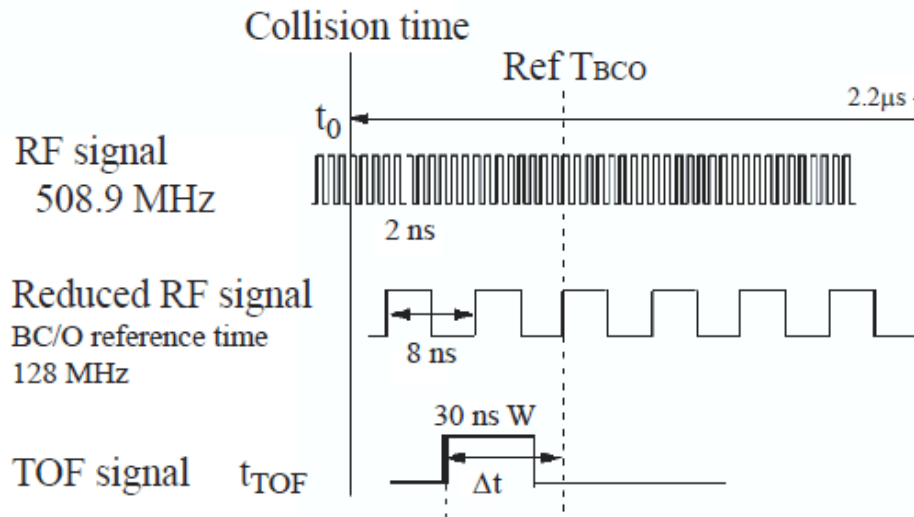
FTSW clock, trigger, programming



16 FTSW

Event Timing

- At Super-KEKB the timing of signals should be **fixed** relative to trigger (system clock)
 - But it is random with respect to 21 MHz derived (Super-KEKB RF clock).
 - t_{hit} from waveform must be combined with t_{FTSW} from CAMAC TDC to align events.
 - $t_{label} = t_{hit} + t_{FTSW}$



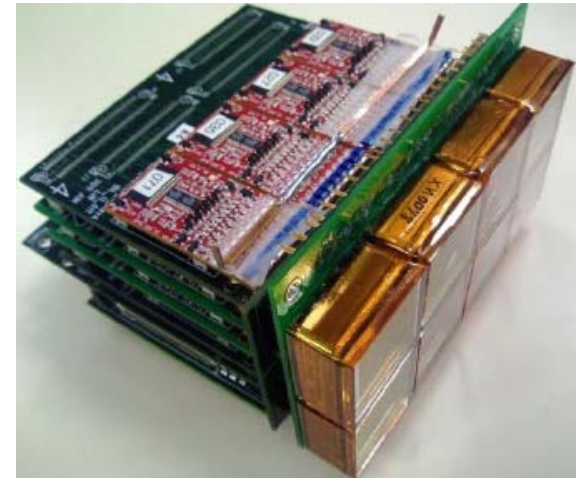
System Synchronization

Crucial to obtain required performance

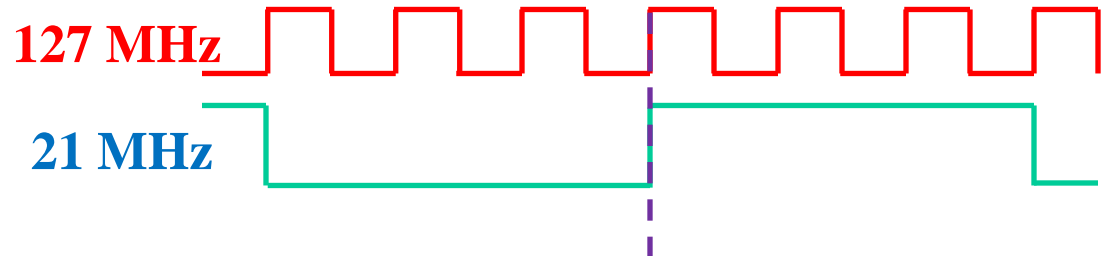
**FTSW (Timing &
Trigger Distribution
board)**



127 MHz clock →
Serial data
(trigger &
synchronization)

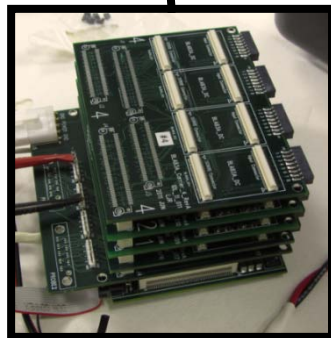
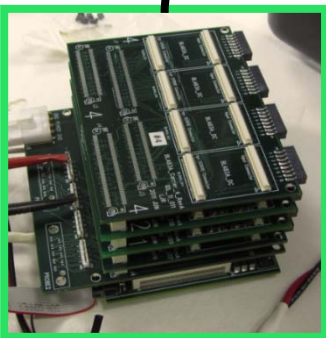


- 127 MHz clock is divided by 6 on front-end module to ~21 MHz
 - This corresponds to sampling rate of ~2.7 GSa/s
 - FPGA uses serial data stream to determine clock phase

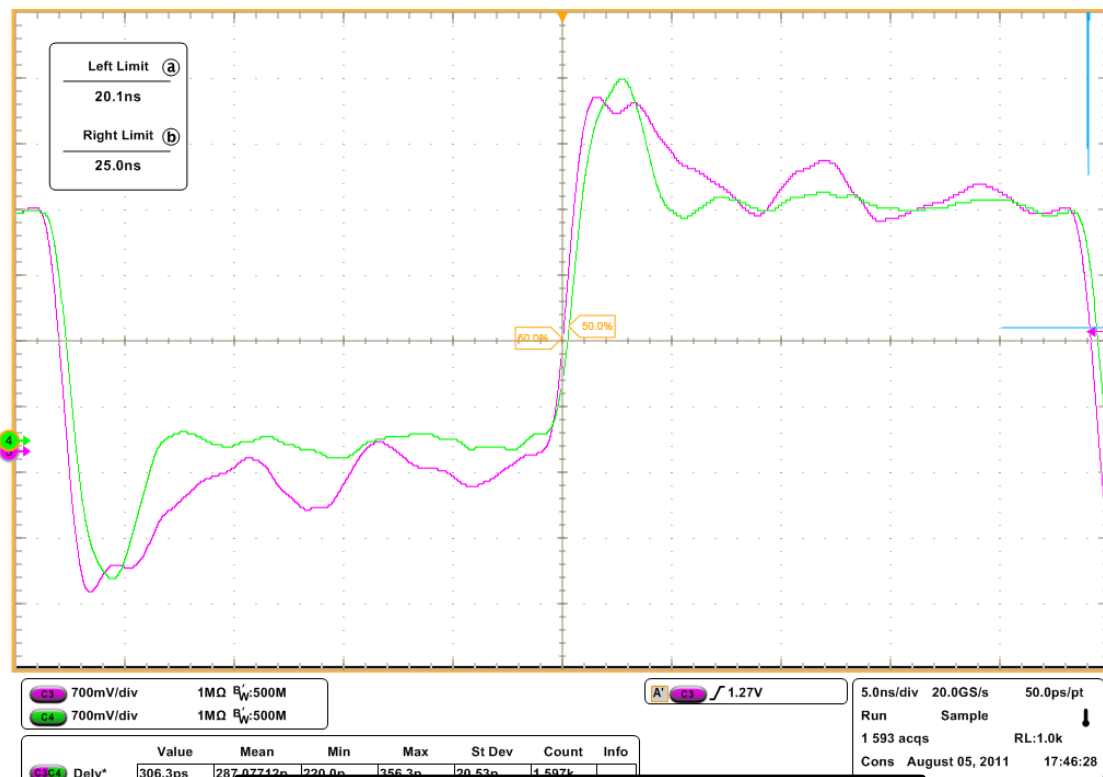


Clock Distribution Performance

- Test results performed as part of the cosmic ray test stand integration at Nagoya Univ in August 2011:

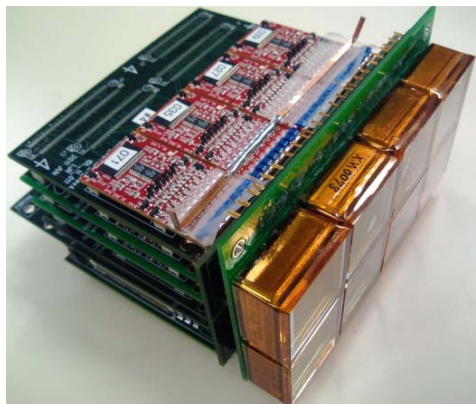


**Measured phase and jitter of
21.2 MHz clock from two
modules
(on oscilloscope)**

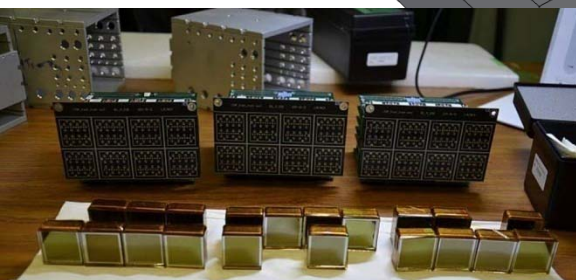
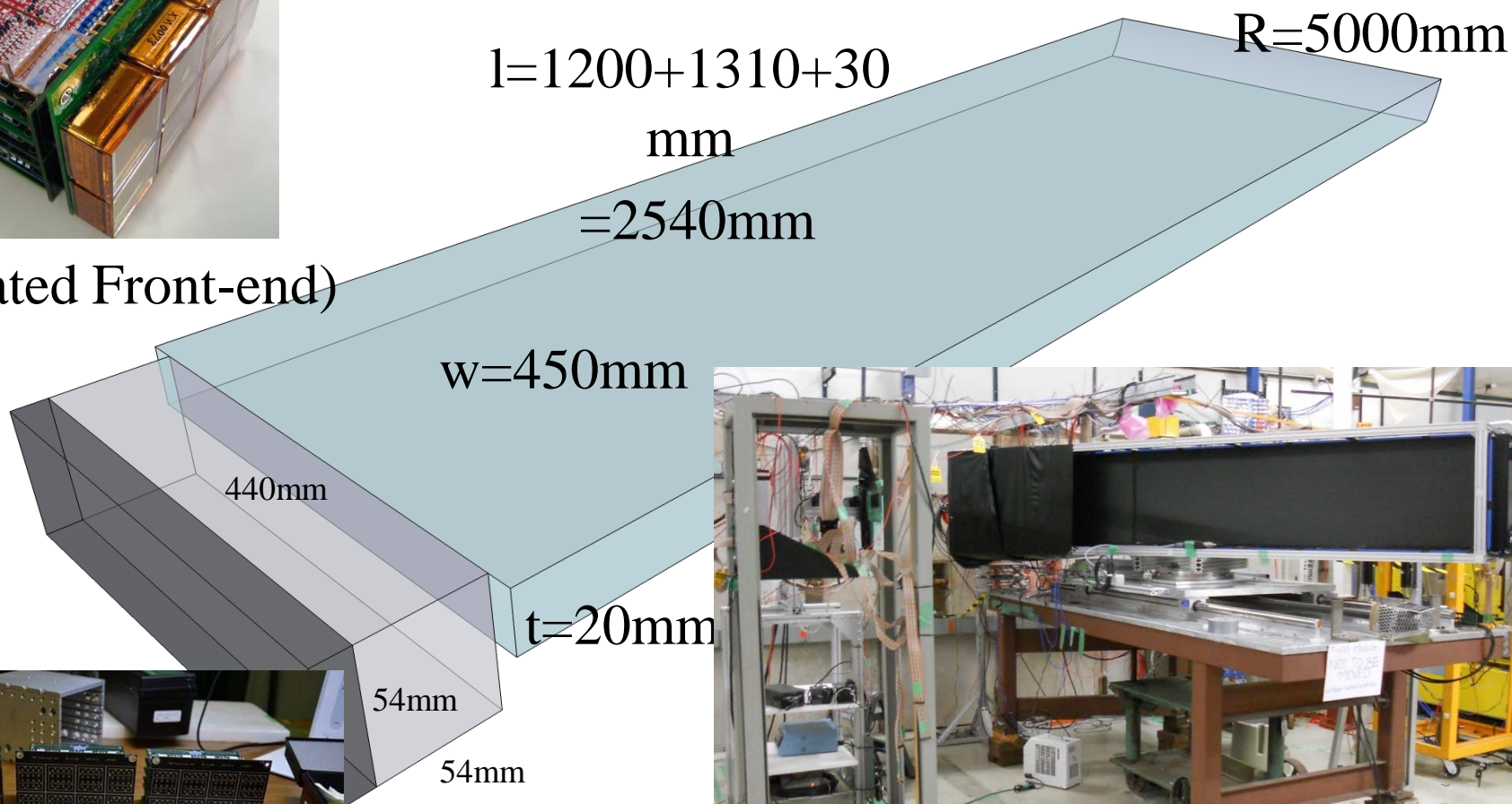


**Clocks are phase-aligned.
→ Measured jitter: 20 ps
RMS.**

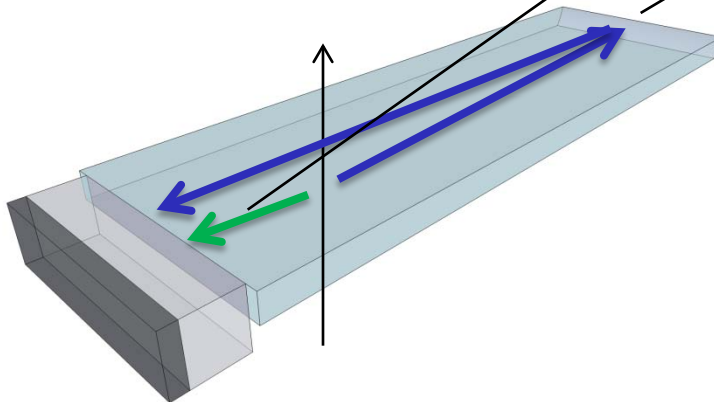
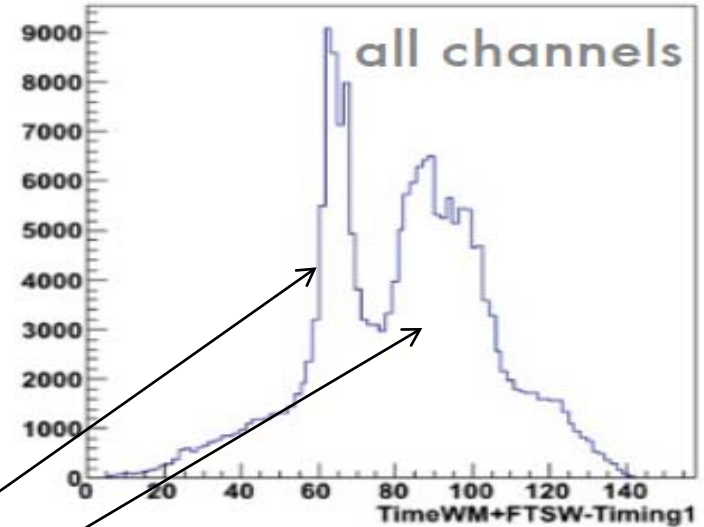
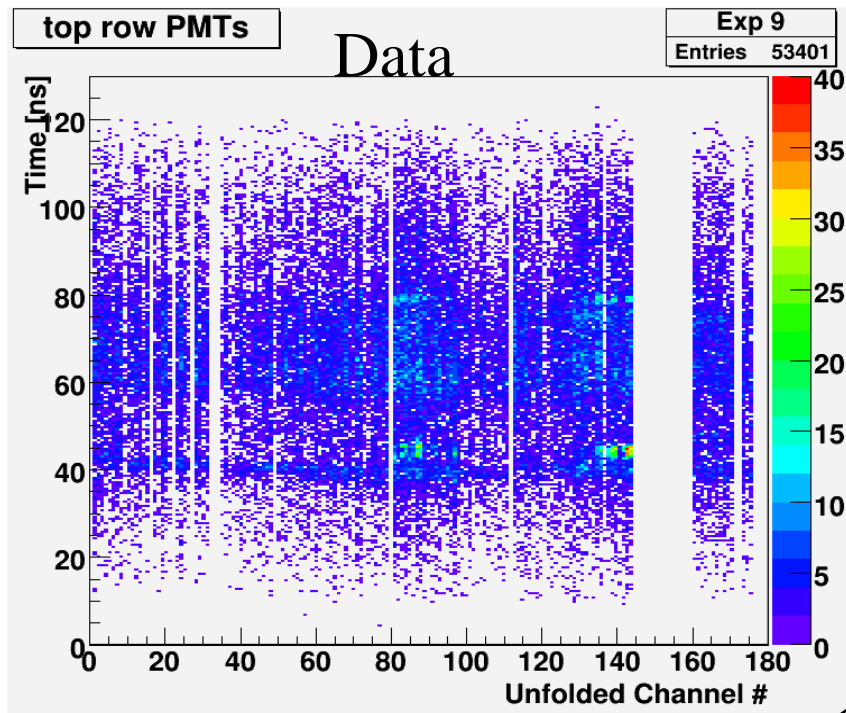
2011-2012 Fermilab Beam Test



(Integrated Front-end)



Hit distribution for normal incidence

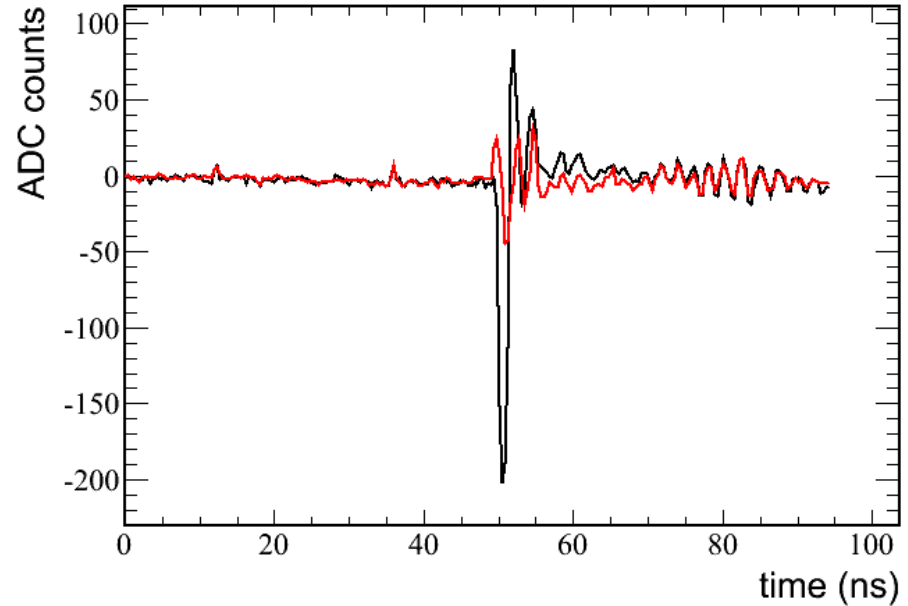
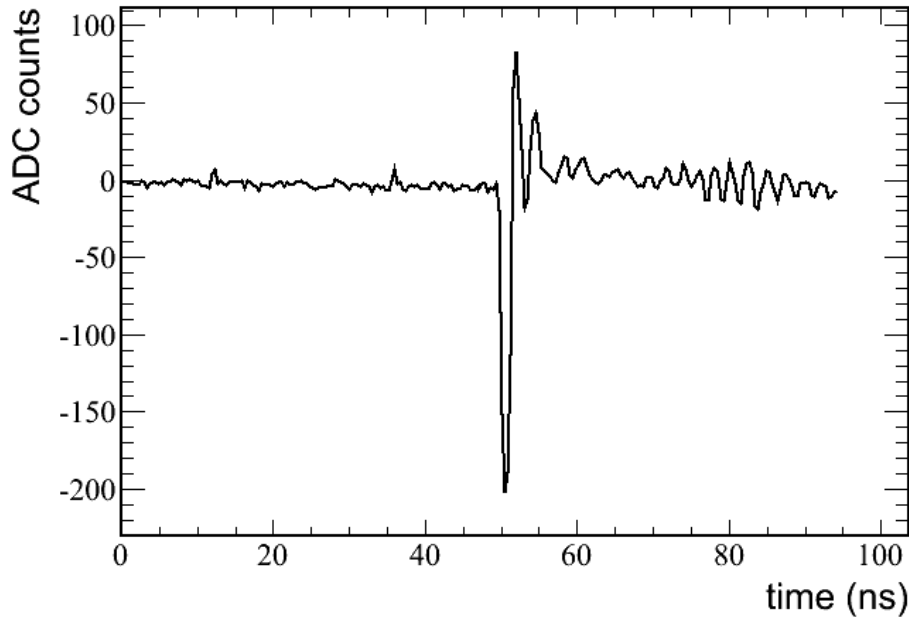


Could see direct photons and mirror-reflected photons.

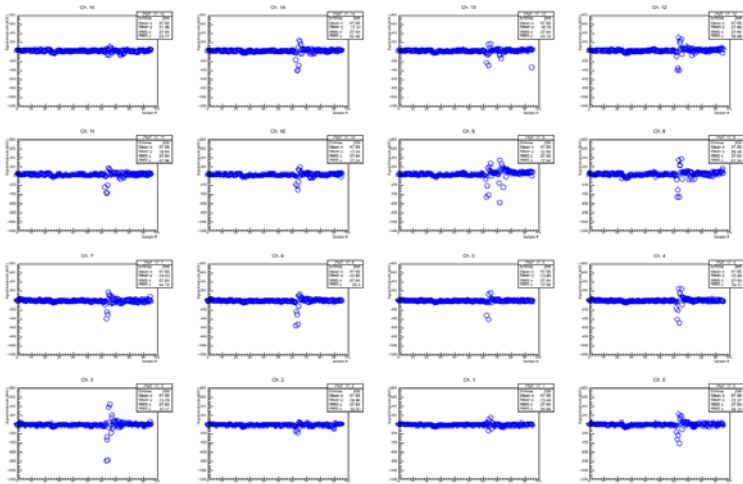
However, there is large background

Veto shower and cross-talk cuts needed

Signal processing



Clean hit (center of Anode pad)

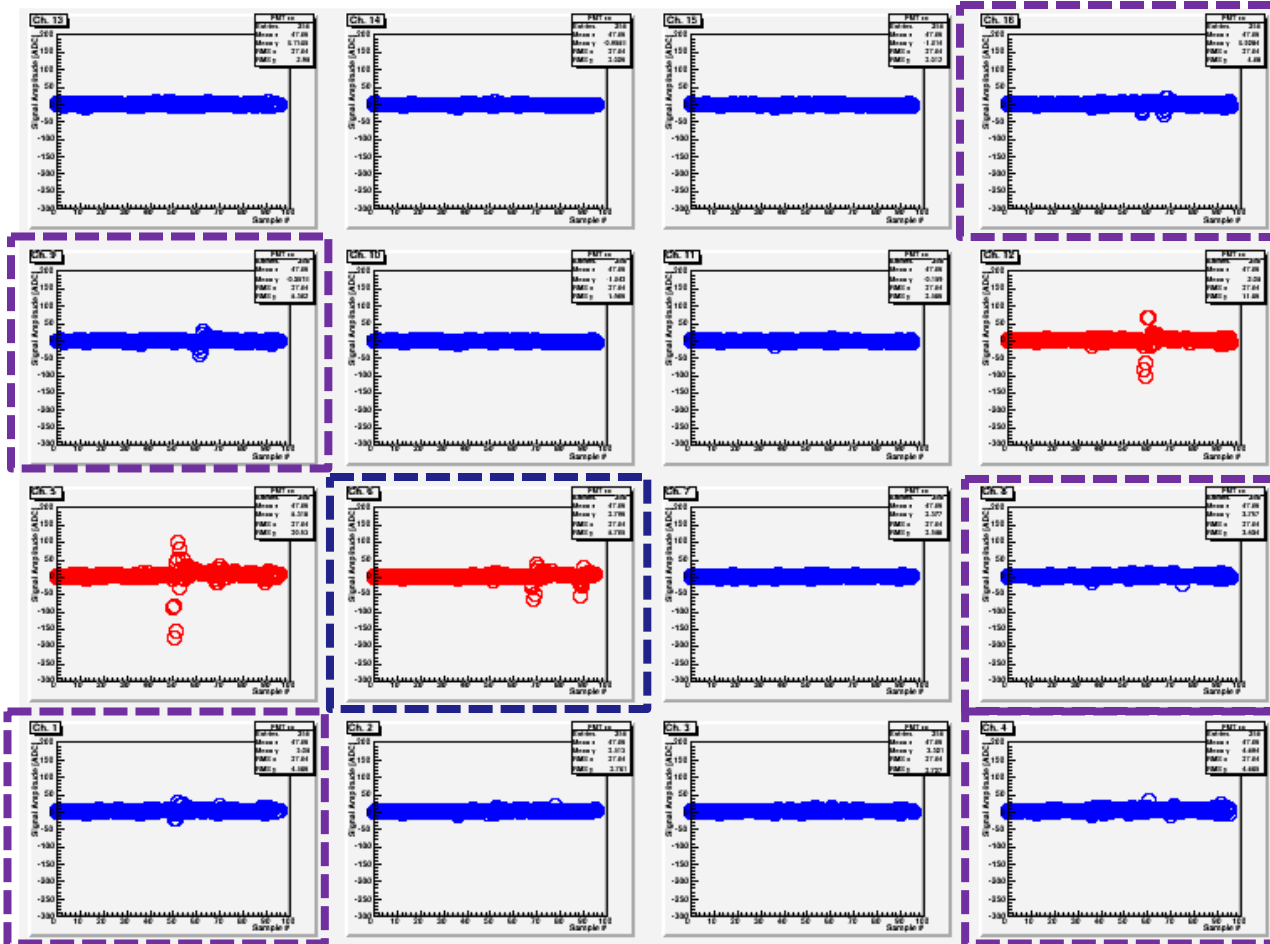


**Depending upon amplitude,
“cross talk” hit (red) ==
remove by filtering**

**Can (in principle) decouple
PMT, wiring & readout x-
talk**

Photon Counting Studies

Example event, waveforms from all channels of one MCP-PMT



Red – waveform with a hit to be counted in total

N_y

Blue – waveform with no hit

Testbed for:

- Ensuring cross-talk or charge sharing events are not double counted.
- Counting double hits.
- Avoiding any artificial digital glitches that might otherwise be counted.

➔ Single p.e. laser studies allow a more controlled environment to check cross-talk from various sources.

Temperature Dependence

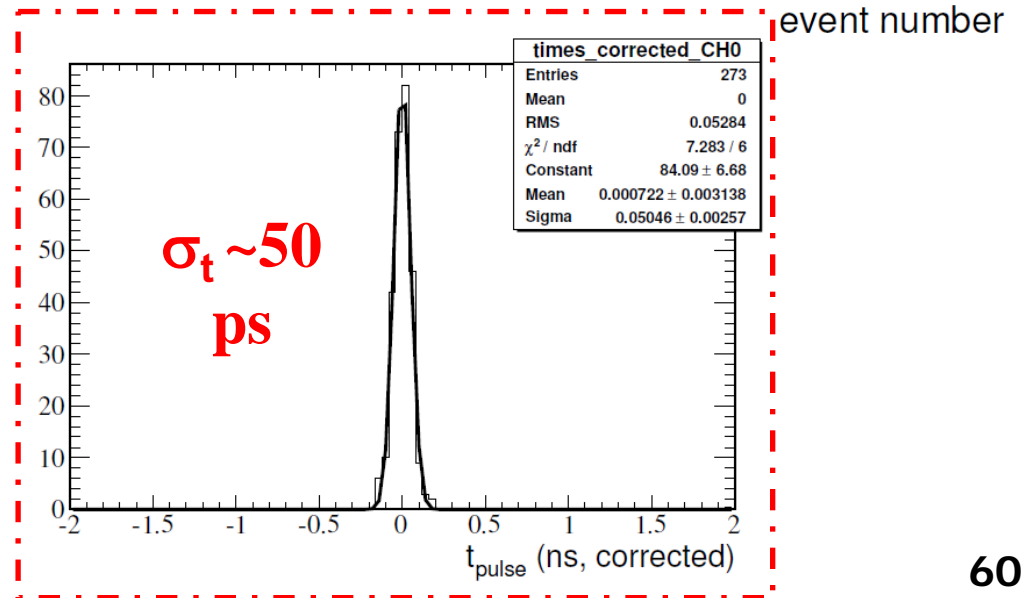
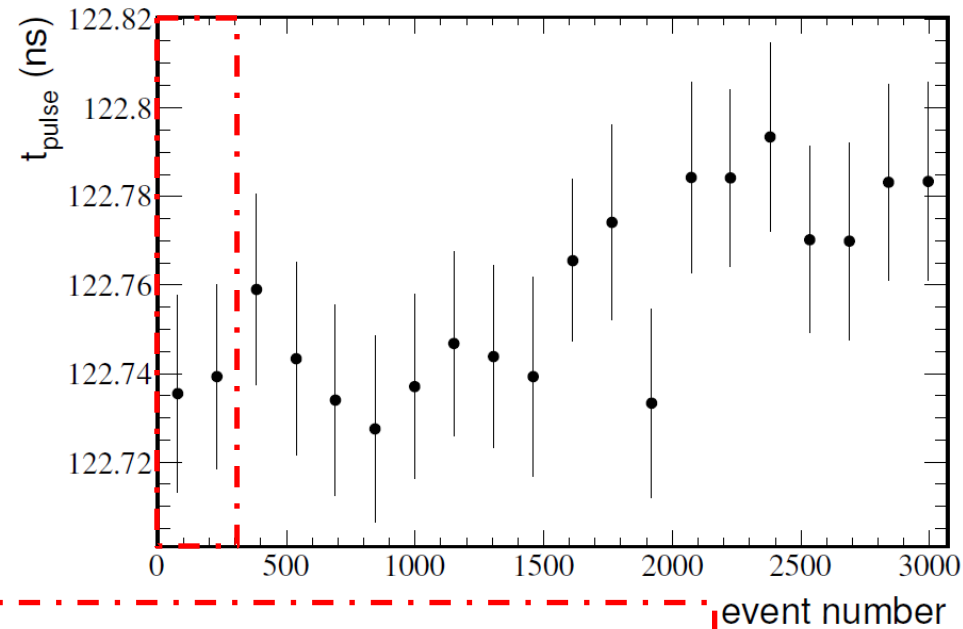
- Timing observed to drift over event number

- Contributions:

- Baseline shifts in waveforms
- Change of time-base with temperature

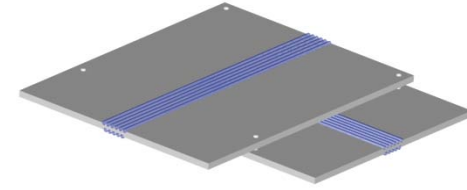
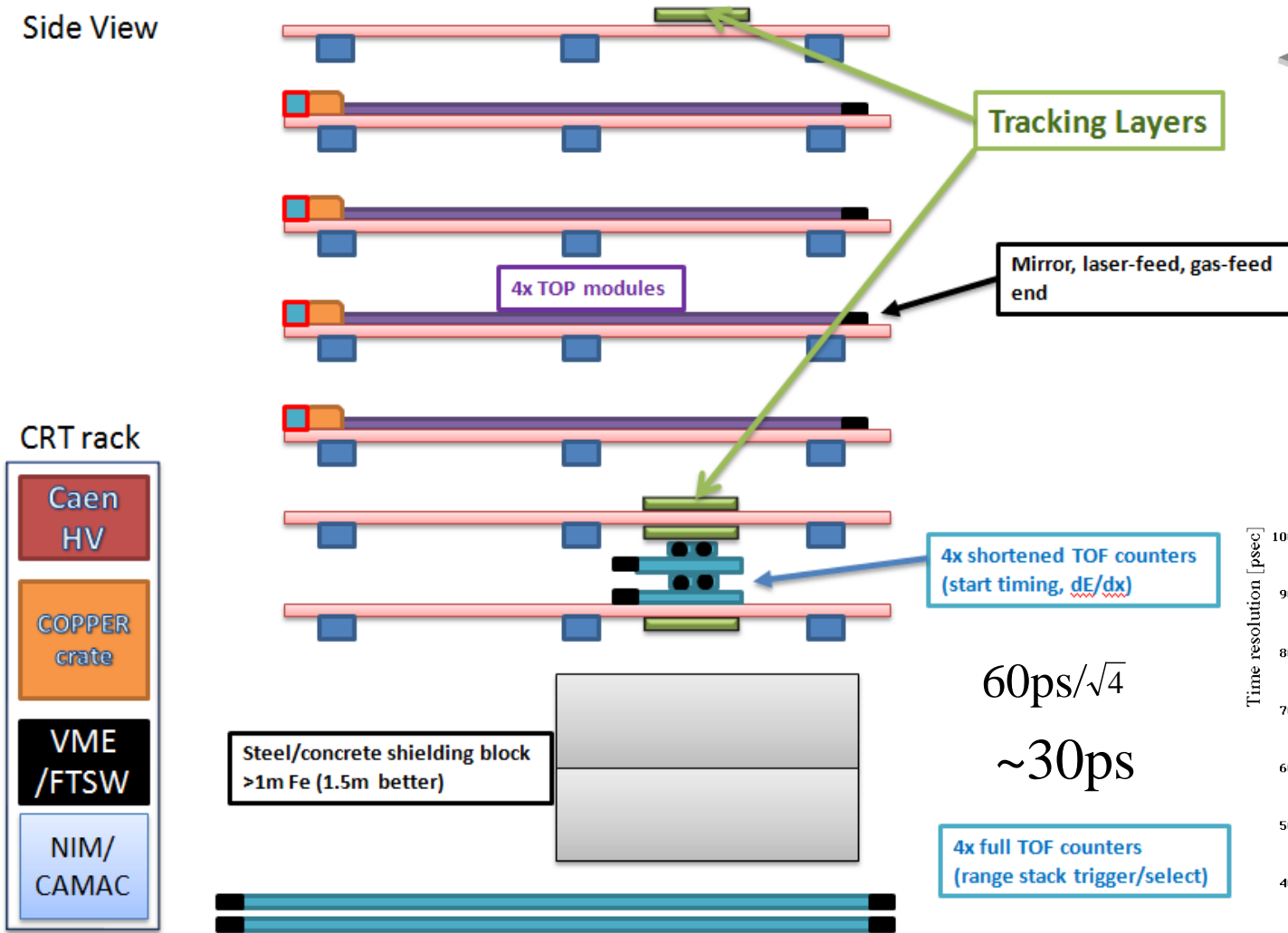
- Timing over limited event region demonstrates improvement in timing resolution by removing these effects

For pulsed channel, hit time vs

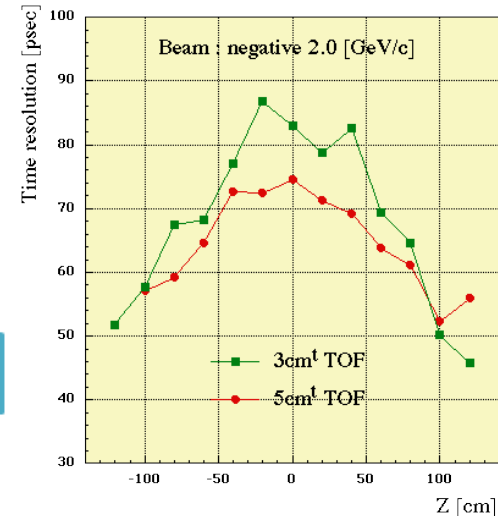


Cosmic Ray Telescope (Fuji Hall, KEK)

Side View



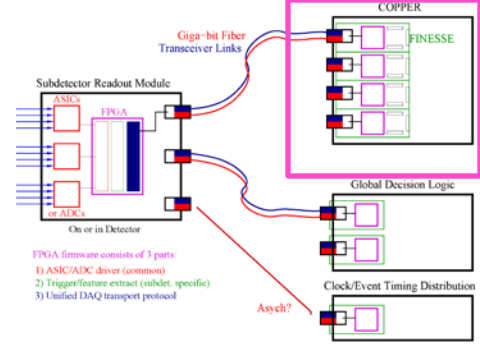
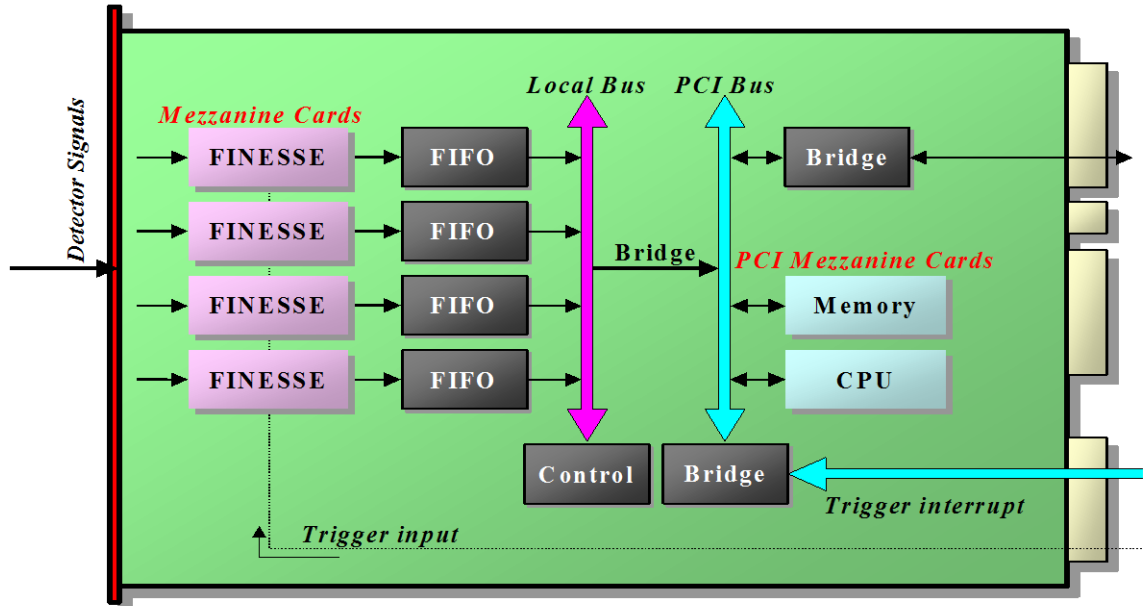
$\sim 1\text{mm}$
resolution
Sci Fi tracker
over
 ~ 2 meters
 $< \sim 1\text{mrad}$



Under construction now: testbed for “final” ASIC,
pre-production electronics

CRT Platform: Back-end processing

Schematic Drawing of the COPPER



Upgraded for Belle II

- COPPER (COMmon Pipelined Platform for Electronics Readout)
- Used in Belle, J-PARC experiments
- FINESSE (Front-end Instrumentation Entity for Subdetector Specific Electronics)

Fast-feature extraction -- beam & CRT

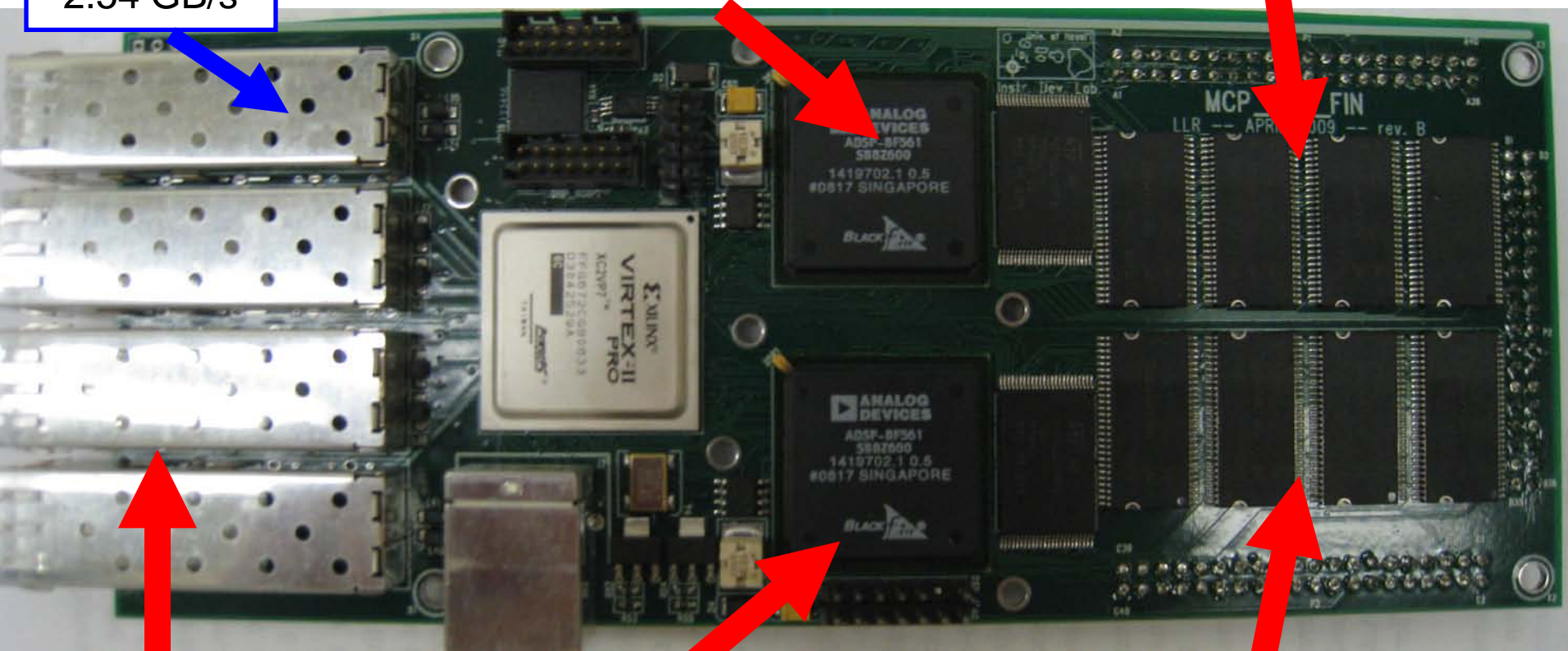
- 500 MHz processor per core
- 32x waveform channels per core
- 60k Waveforms/s benchmarked

DSP_FIN

2.54 GB/s

Dual Core DSP

128 MB SDRAM



4x Fiber Optic Connections

Dual Core DSP

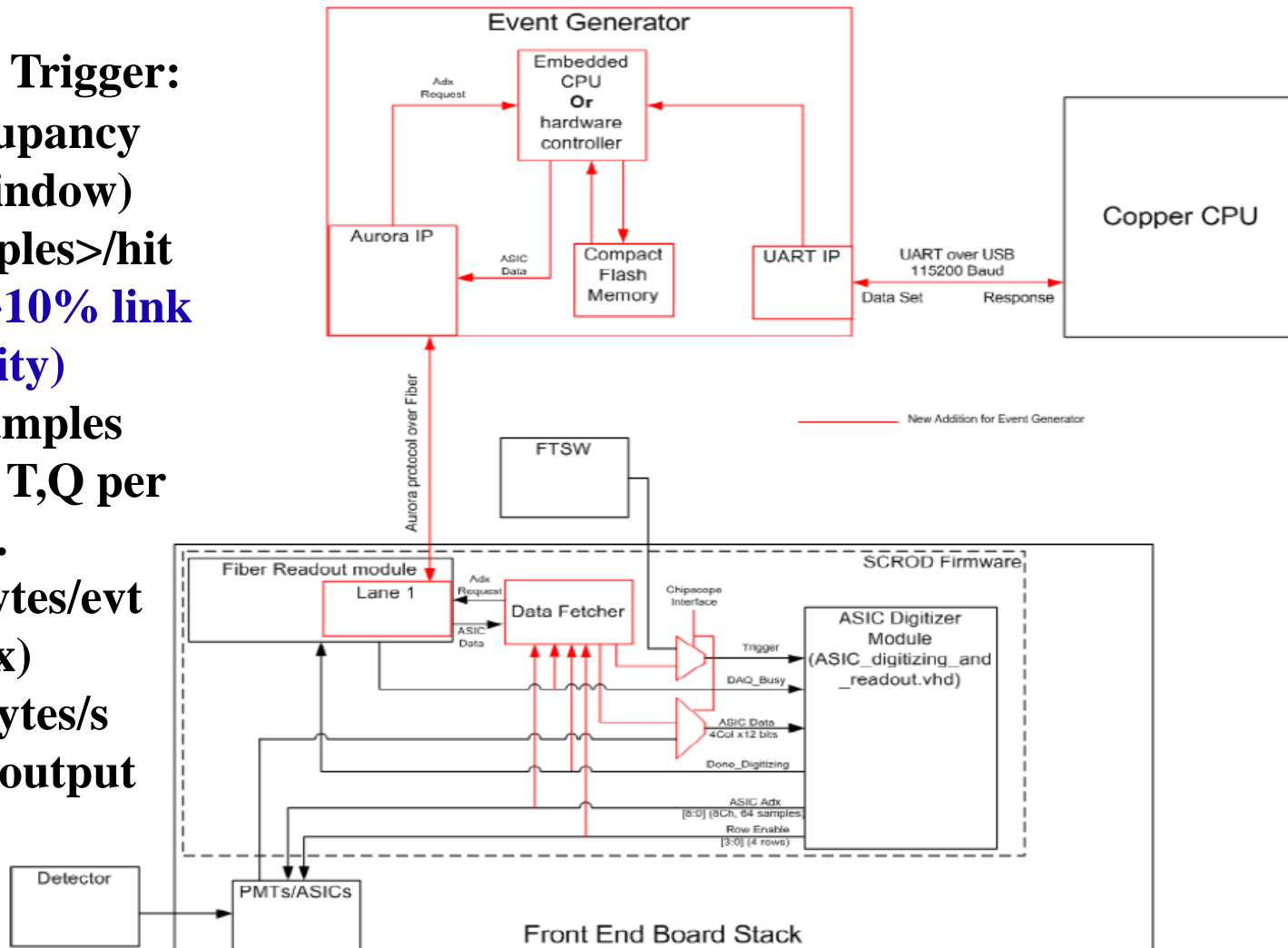
128 MB SDRAM

Data Reduction Exercises

Event Generator Design

“full speed” testing

- 30kHz L1 Trigger:
2.5% occupancy
(100ns window)
- <100 samples>/hit
- 0.3Gbps (~10% link capacity)
 - ~100 samples reduced to T,Q per p.e.
- Few kBytes/evt (max)
 - 13 Mbytes/s expected output



Belle II TOP Readout Status

- **IRS3B fabricated** (“final ASIC, if no changes needed”)
- Next generation control firmware in development v.2 fDIRC CRT; v.3 IRS3B, backend processing
- Redesign, fab of next generation board stack
 - Improved HV, cooling
 - Feedback control, in-situ calibration
 - Amplifier options being studied (N.B.: 5×10^5 gain)
- Experience with confirming prototypes by end of 2012, “pre-production” early 2013
- Production in late 2013-2014
- **Installation, commissioning and operations: 2015-2016**

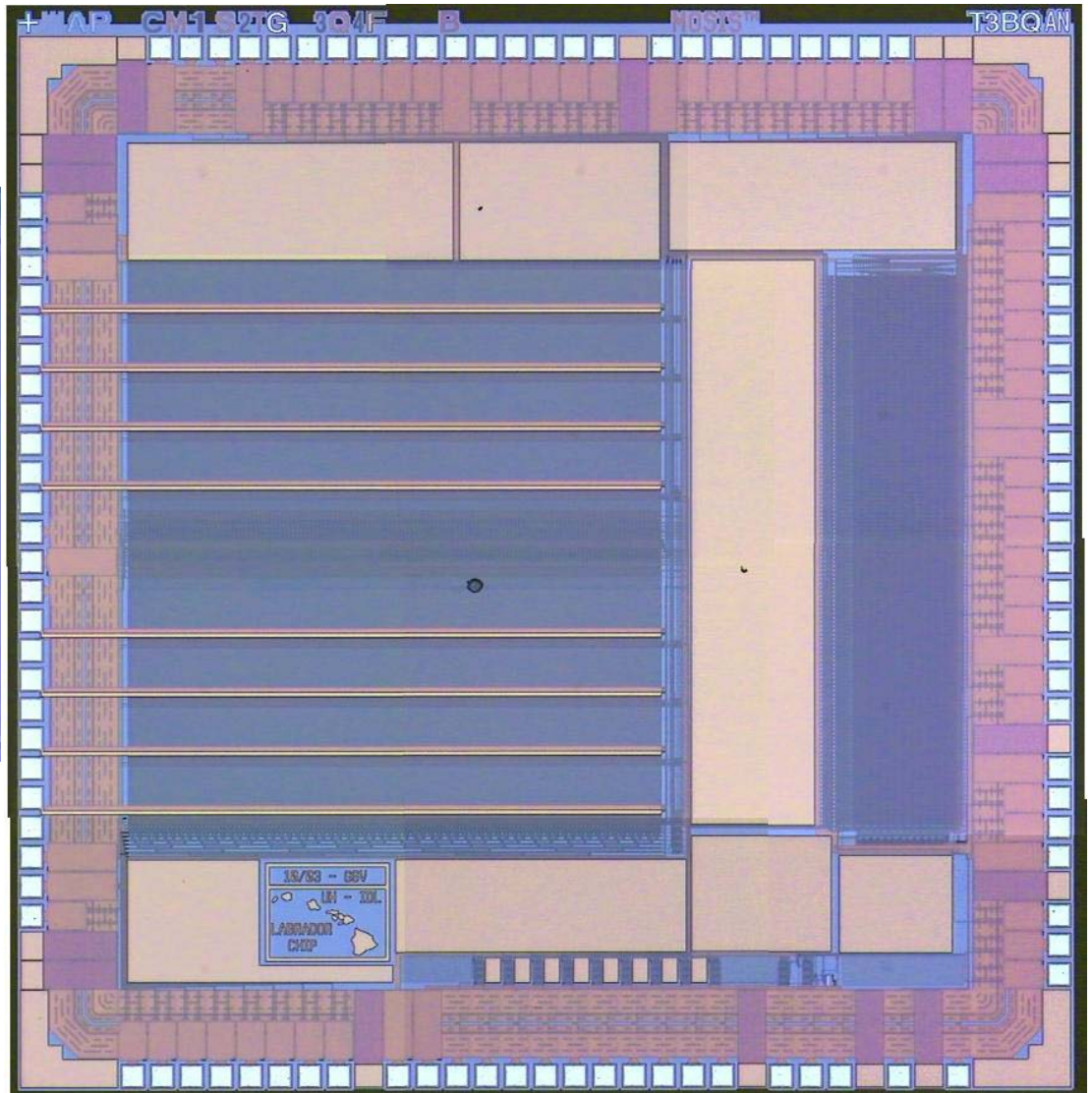
Summary

The “Giga” Era of Instrumentation is here

- Enables whole new ways of instrumenting detectors
- Commodity components and processes open whole new opportunities



Back-up slides

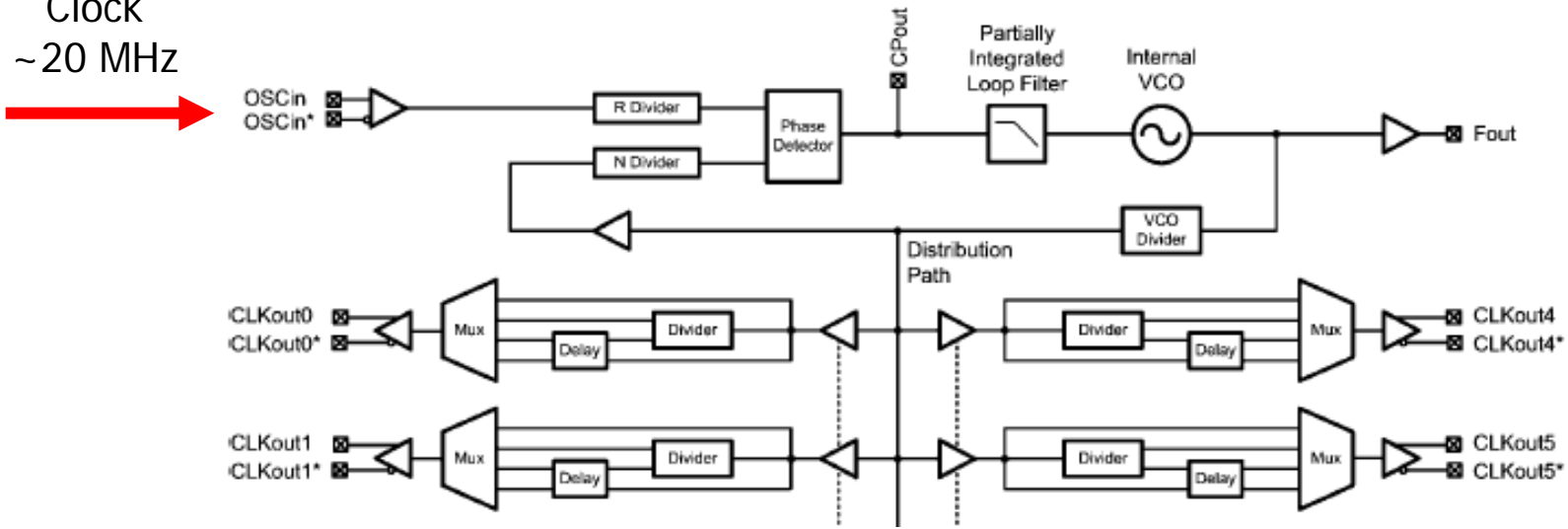


Timing Big Systems I

LMK03000 Clock Conditioner
(National Semiconductor)

Jitter: 400 fs

Global
Clock
~20 MHz



Reference
Clock for
DRS4 PLL
2.5 MHz

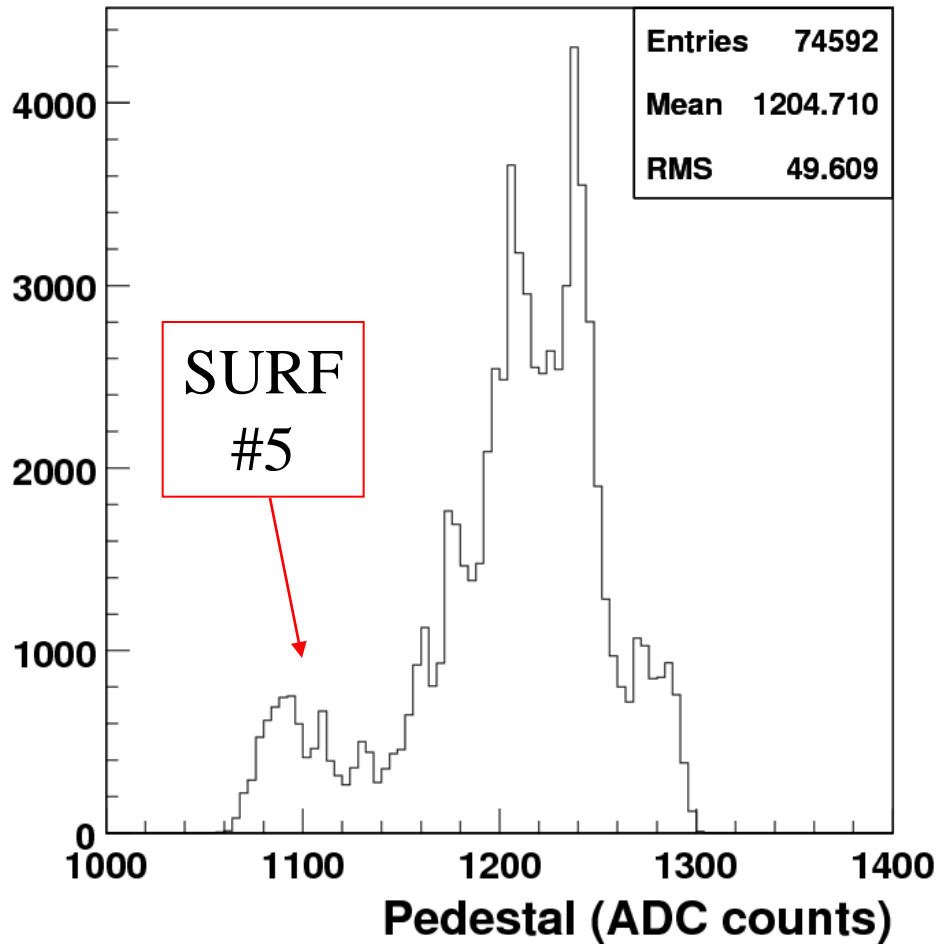


Reference
Clock for
timing
channel



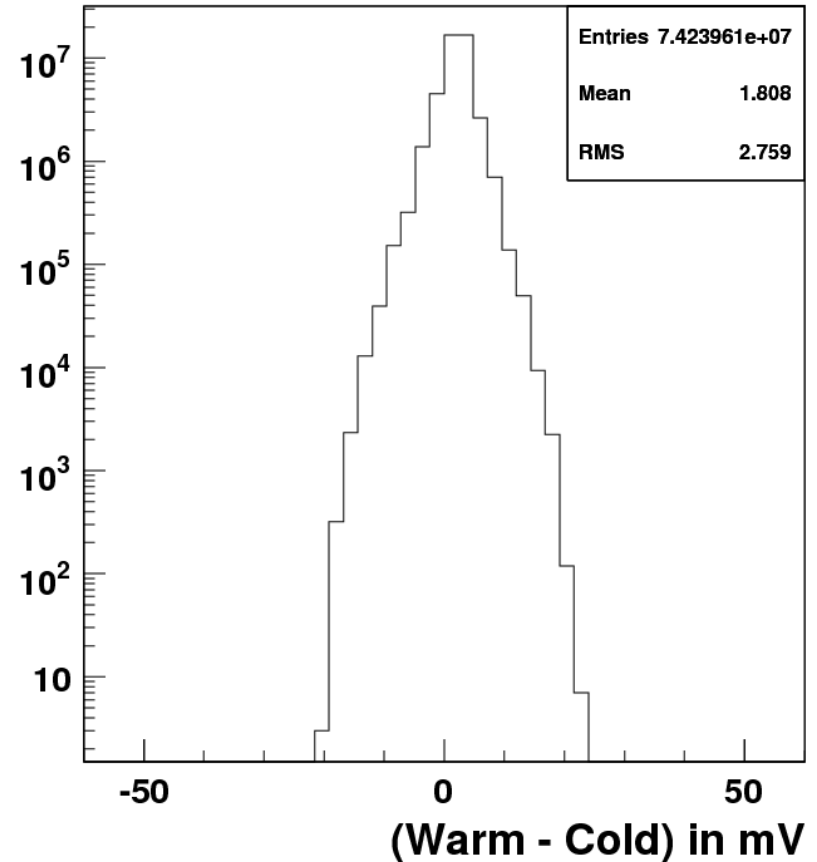
Pedestal and Pedestal Stability

Pedestal Distribution



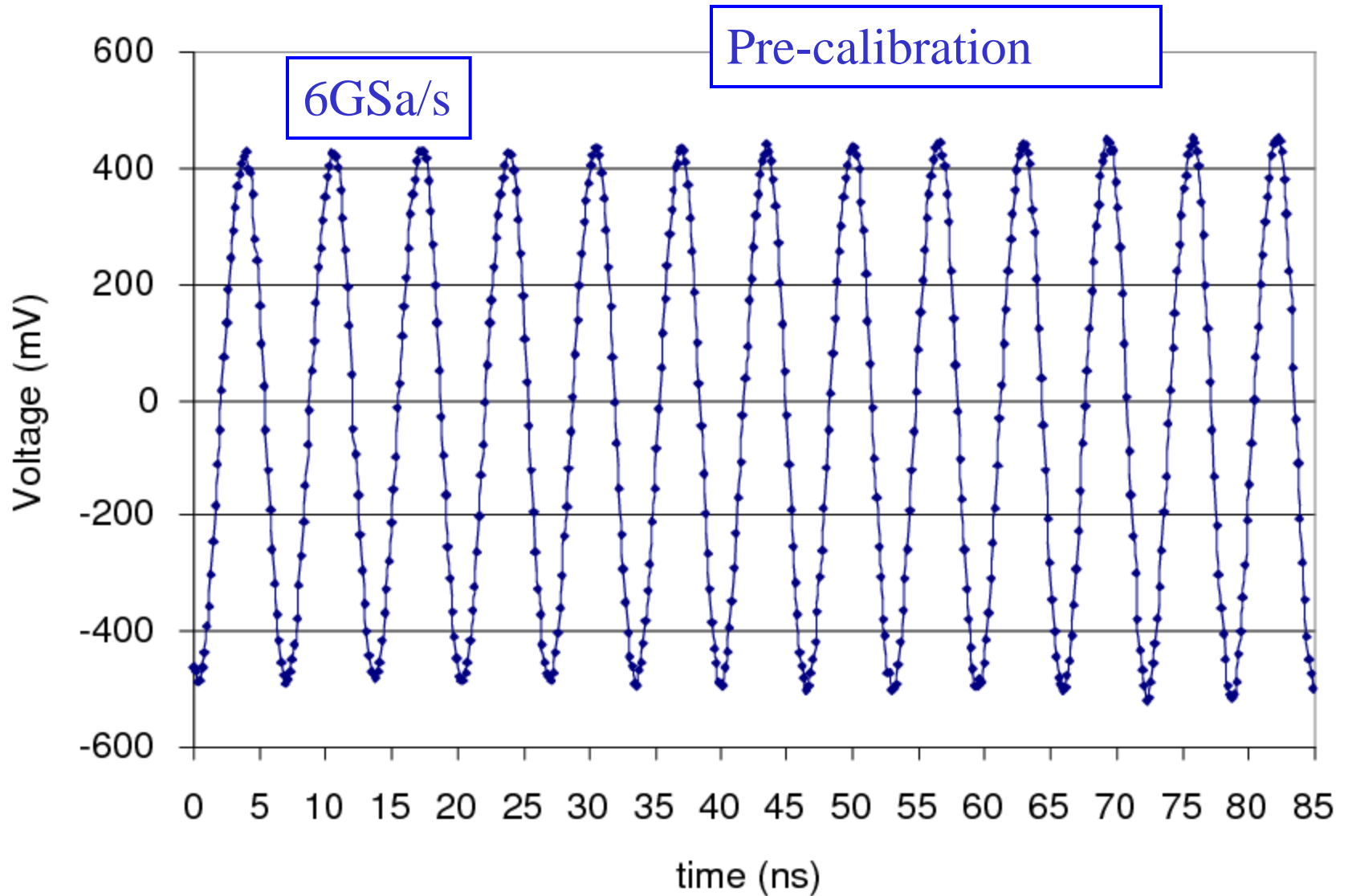
- AC coupled input

Pedestal Stability

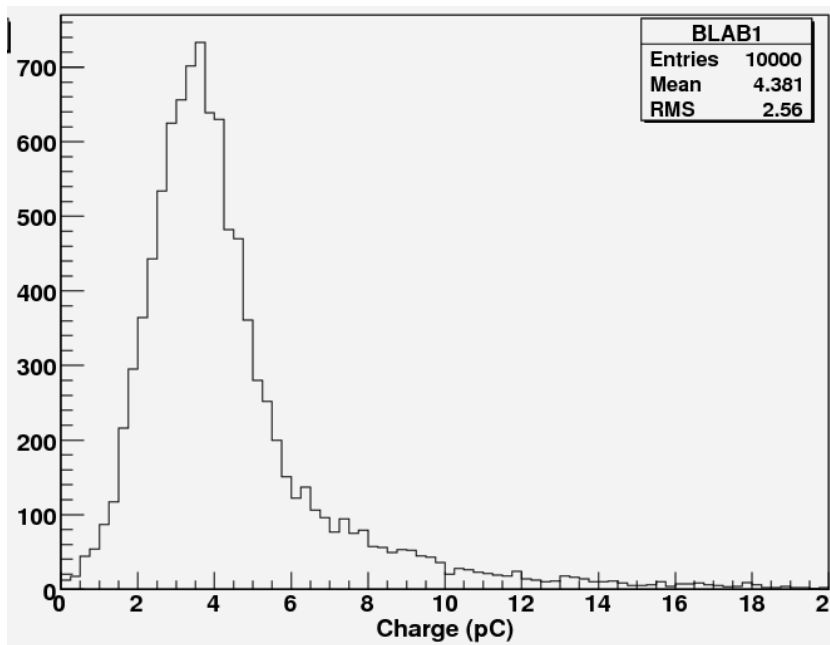


$\Delta T = 17C$ ($\delta t \sim 24$ hours)
 ~ 0.052 mV/C

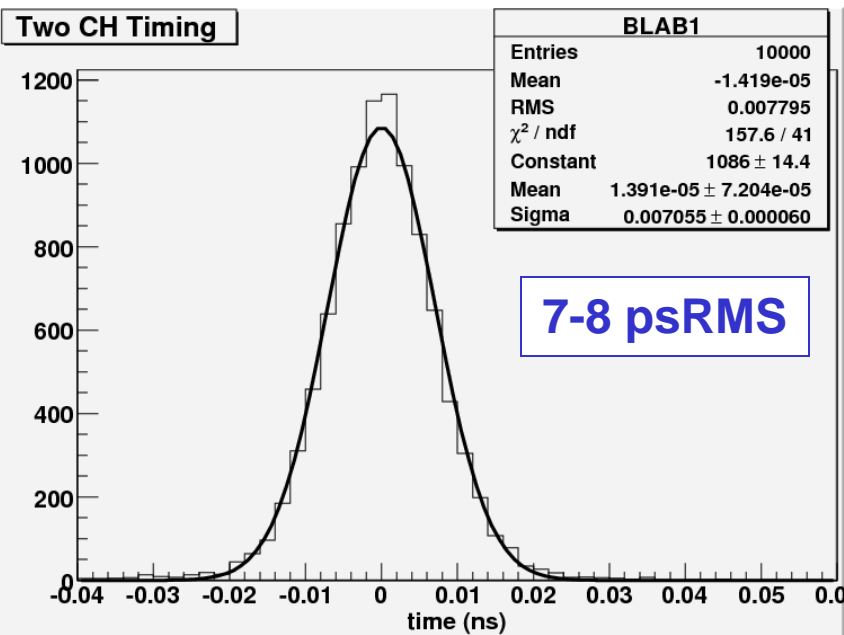
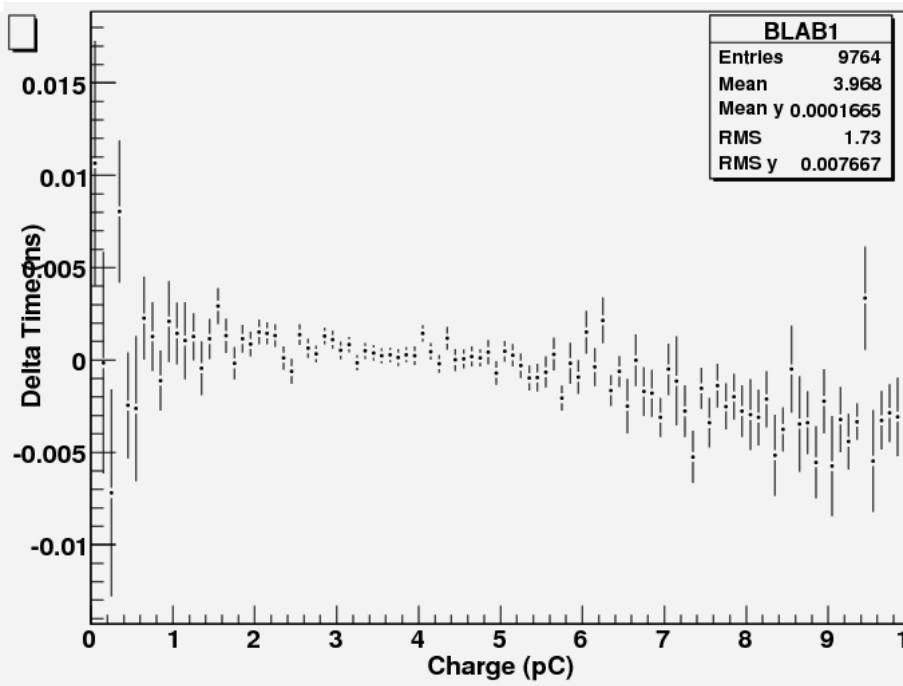
125MHz sine wave



Real MCP-PMT Signals (with BLAB2)



Residual Time Walk



Rather robust for amplitude invariant signals, TOF still hard, but can shape extract

Simulated Performance vs. SNR

300MHz ABW, 5.9GSa/s

