高速飛跡検出のための技術開発

奥村恭幸

University of Chicago, Enrico Fermi Institute

Fermi National Accelerator Laboratory

トークの概要

パート１

エネルギーフロンティアでの高速飛跡検出の重要性

パート２

高速飛跡検出のコンセプト

Associative memory による“並列化”

ATLAS FastTracker System (通称 FTK) の紹介

パート３

最近の技術開発の紹介

ATCA backplane system for “Data Formatter”

3D CAM for “track finding”

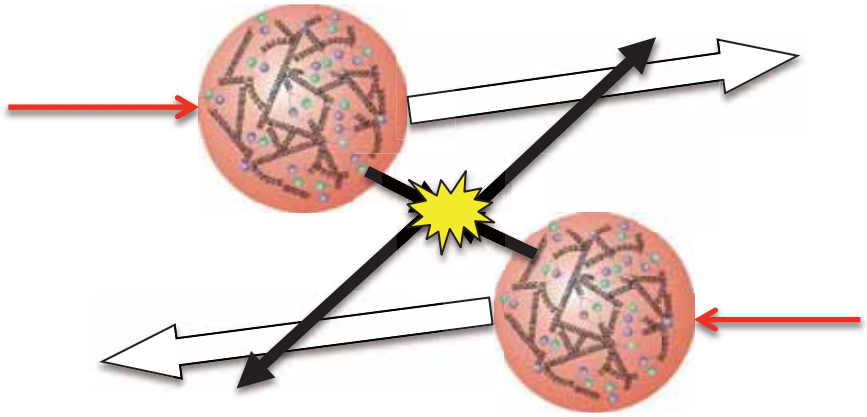
Graphical Processing Unit (GPU) for “track fitting”

パート１
エネルギーフロンティアでの高速飛跡検出の重要性

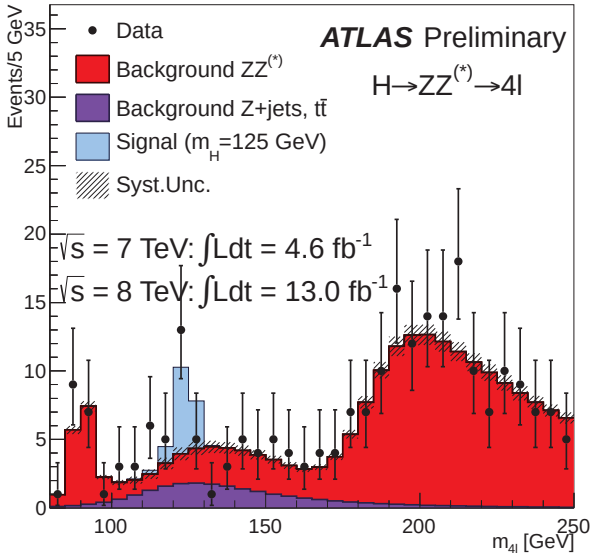
Large Hadron Collider

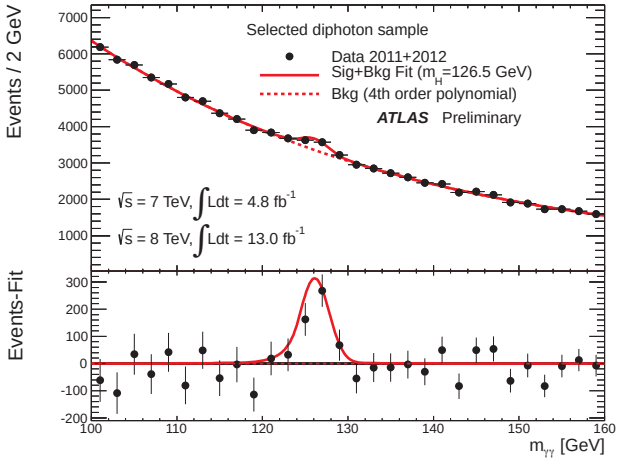
- *世界最高エネルギーの陽子・陽子衝突型加速器*
  - 運転パラメータ
    - 4 TeV + 4 TeV
    - L=7.6/nb/s
    - L=22 fb (2012)
    - N_{ppb}: 1.6×10^{11}
    - N_{bunch}: 1380 (50ns spacing)
    - ε: 2.2-2.5 um
    - β*: 0.6 m

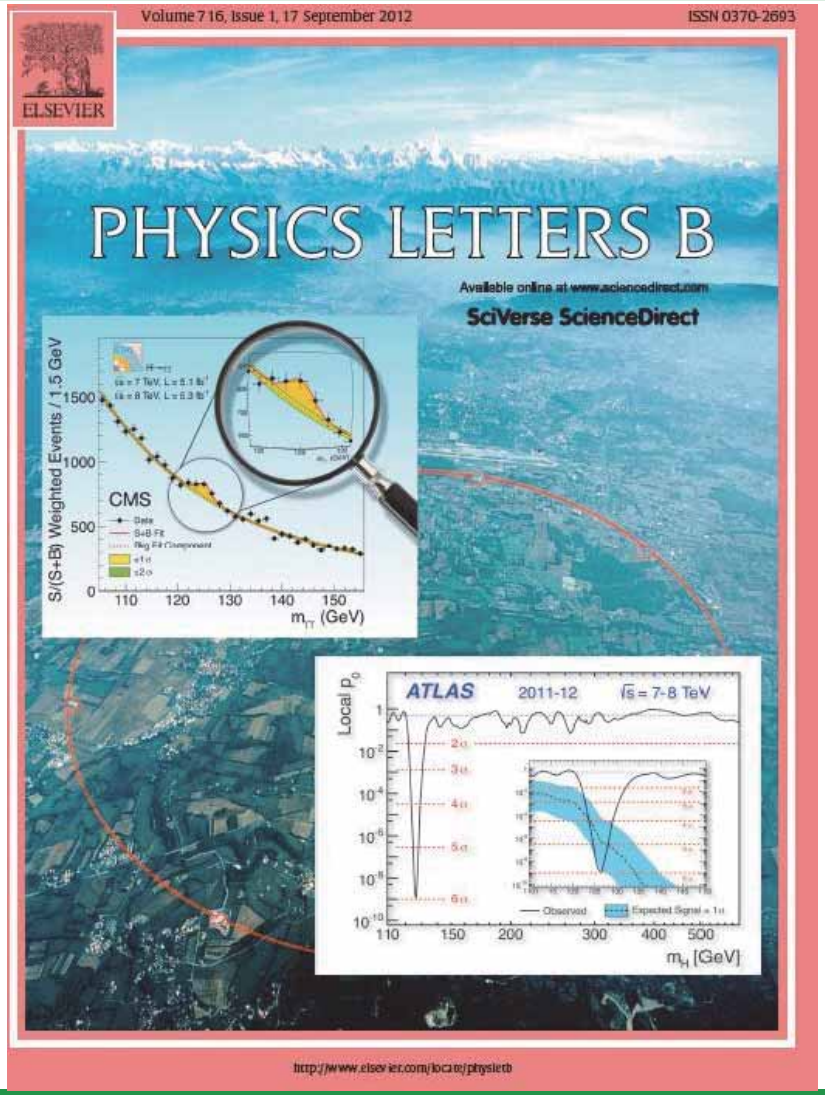
- *陽子陽子衝突*
  - パートン同士の衝突
    - 強 >> 電弱 >>> .. >> 重力
  - $\sqrt{\hat{s}} = 2\sqrt{x_1 x_2} p_{\mathrm{proton}}$



ヒッグス粒子の発見 @ ATLAS & CMS







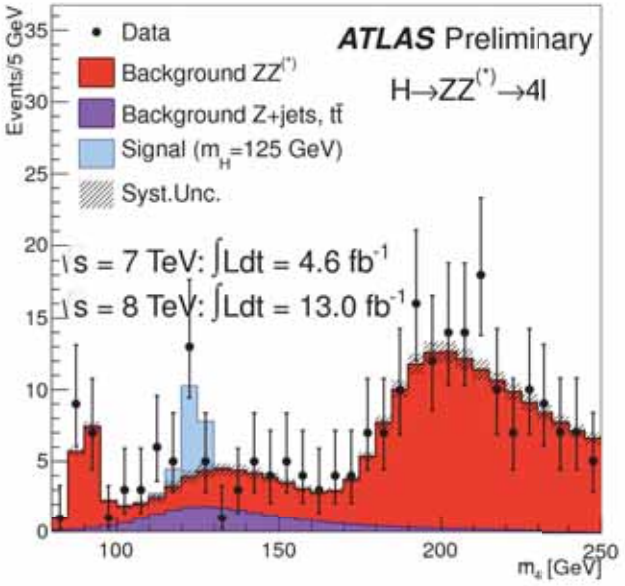
エネルギーフロンティア物理の目標

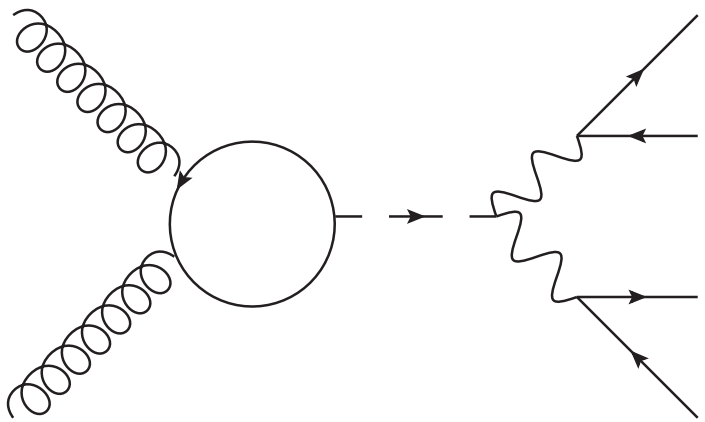
ラージハドロンコライダーでの
フェムトバーンレベルの物理現象の理解

($fb = 10^{-15} b = 10^{-39} cm^2$)

✓ヒッグス粒子の性質の解明

✓標準模型を超える物理現象（超対称性）の探索





$\sigma \times \mathrm{BF}(h \to ZZ^* \to 4\ell) = 3$ fb

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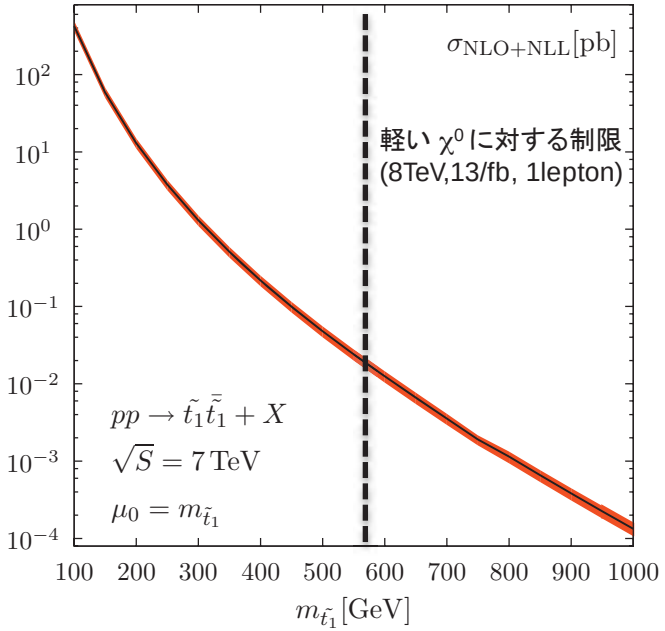
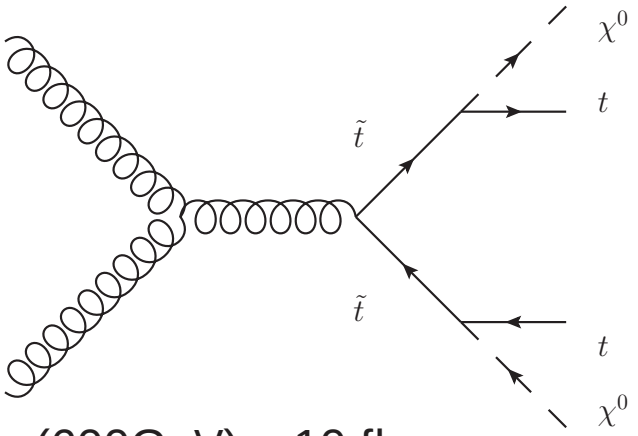




σ(600GeV) ~ 10 fb
σ(800GeV) ~ 1 fb
σ(1TeV) ~ 0.1 fb

目標設定

fb の物理過程の精密測定を遂行可能な
年間 100/fb を測定可能なハドロンコライダー

最高ルミノシティ L = 30 /nb/s (=3x10^{34}/cm^2/s)

(参考 2012 年度実績) L= 7.6 /nb/s で年間 20/fb

– 全非弾性散乱断面積 (Soft QCD) : 80mb
  - (S/B = 1fb/100mb ~ 10^{-14})
– イベント頻度 L×σ = 30/nb/s × 80mb = 2.4GHz

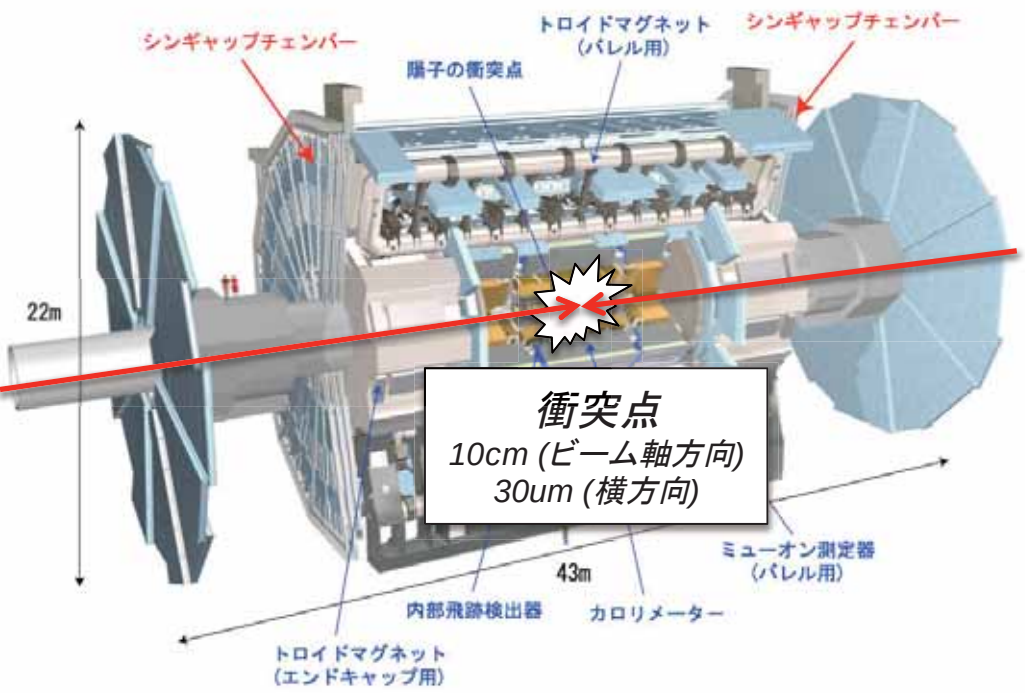
(参考 : 25ns バンチ交差頻度 : 30MHz (空バンチを考慮), ~80衝突/交差)

高イベントレート下 (パイルアップ)で
耐えうるデータ収集系の確立


ATLAS 検出器
(1/3 scale by Josef Kristofoletti)

ATLAS 検出器

Tracking :	Pixel, Silicon Strip, Transition Radiation Tracker
Calorimeter :	LAr & Scintillator
Muon :	Drift Tube, Resistive Plate Chamber, Thin Gap Chamber
(Magnets :	Solenoid (2T) & 3 Troids (2Tm-8Tm))



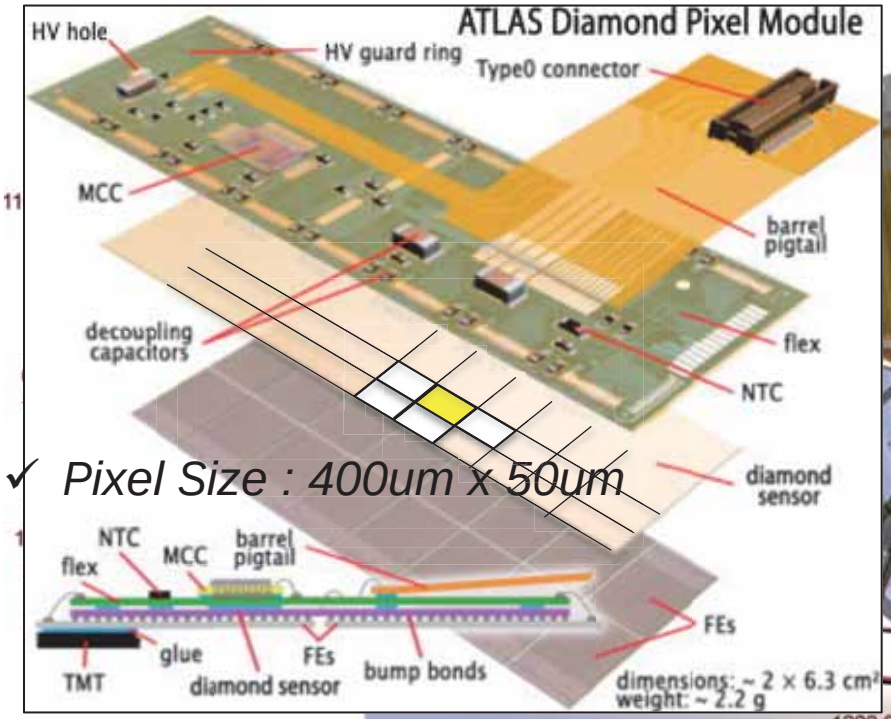
Objects Reconstruction

- ✓ electrons
- ✓ photons
- ✓ muons
- ✓ hadronic taus
- ✓ jets
- ✓ b-jets
- ✓ missing ET

Trigger

✓ Level 1 :	75000 Hz
✓ Level 2 :	6000 Hz
✓ Event Filter :	600 Hz

Pixel 検出器

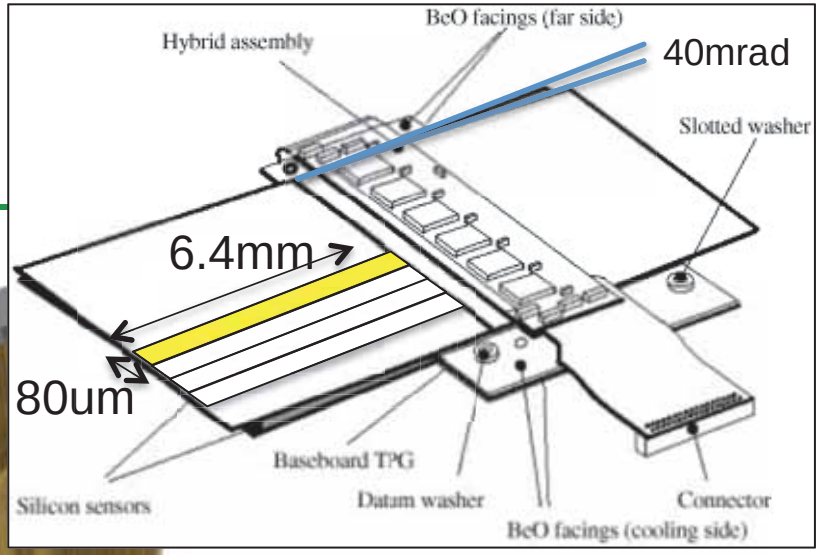


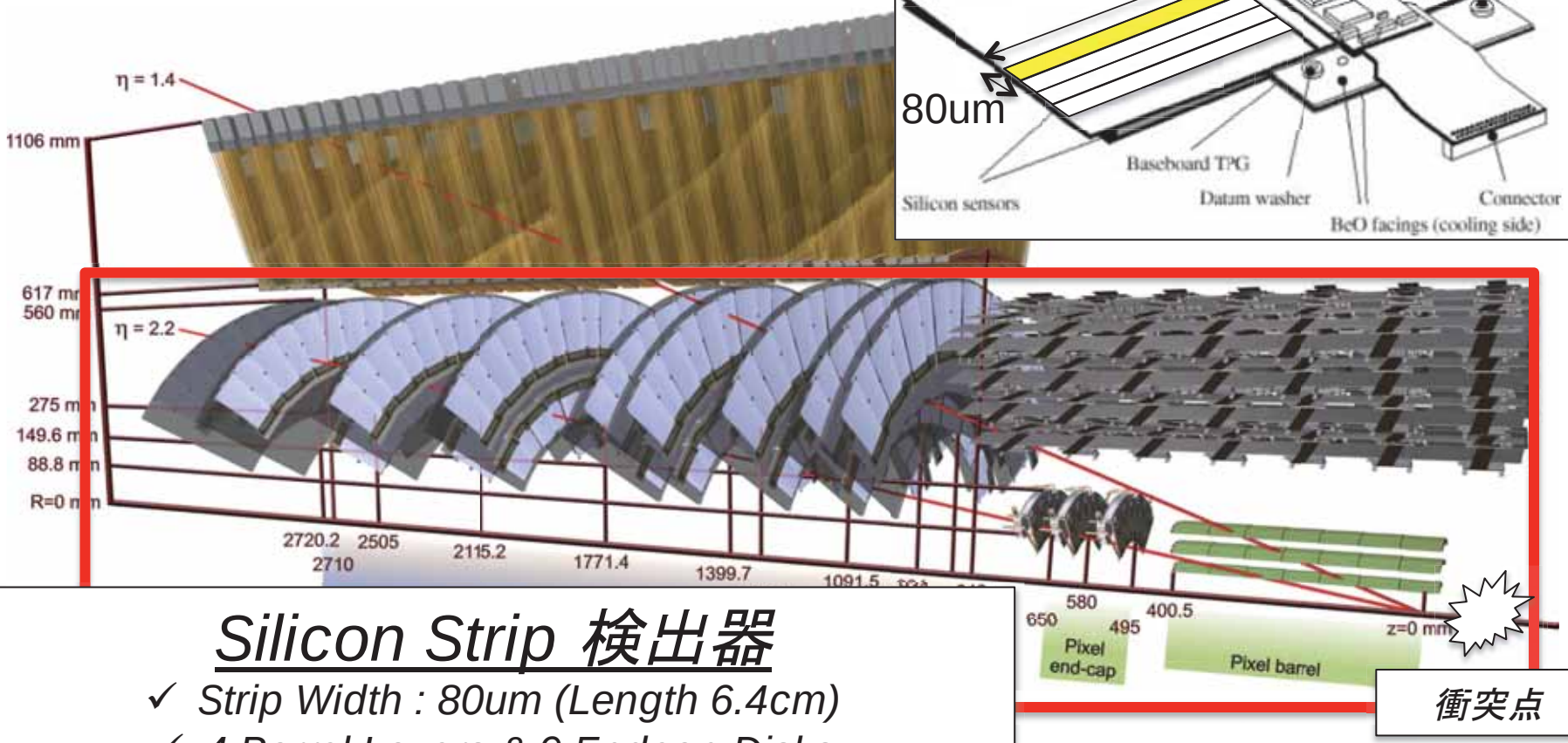
✓ *Pixel Size : 400um x 50um*

Silicon Pixel 検出器

- ✓ *Pixel Size : 400um x 50um*
- ✓ *3 Barrel Layers & 3 Endcap Disks*
- ✓ *80.4 Million Channels*
- ✓ *Thickness: 250um (20,000 e-hole pairs)*

Silicon Strip 検出器



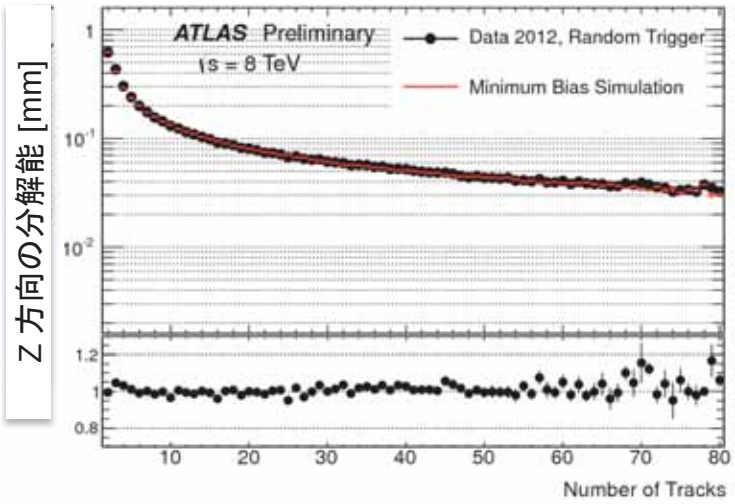


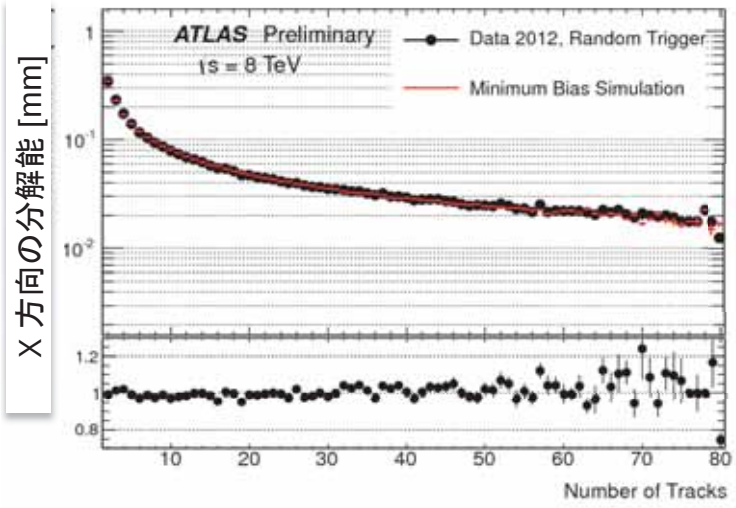
Silicon Strip 検出器

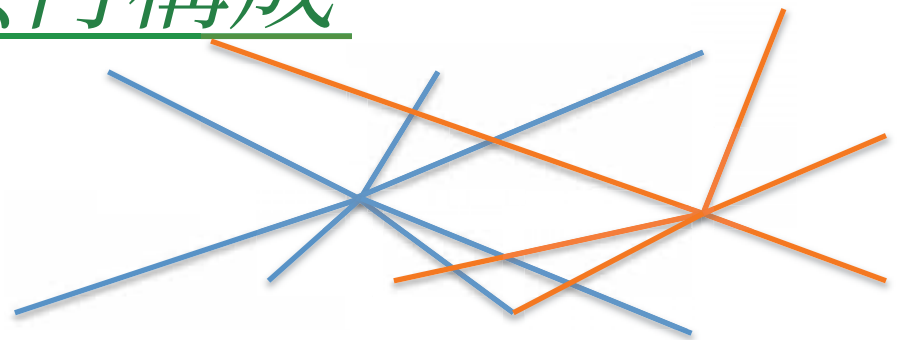
- ✓ *Strip Width : 80um (Length 6.4cm)*
- ✓ *4 Barrel Layers & 9 Endcap Disks*
- ✓ *Stereo angle : 40mrad (2D-position determination)*
- ✓ *6.3 Million Channels*
- ✓ *(doublet of stereo and axial)*
- ✓ *Thickness: 285um (23k e-hole pairs)*

内部飛跡検出器

- 飛跡検出 & 衝突点再構成



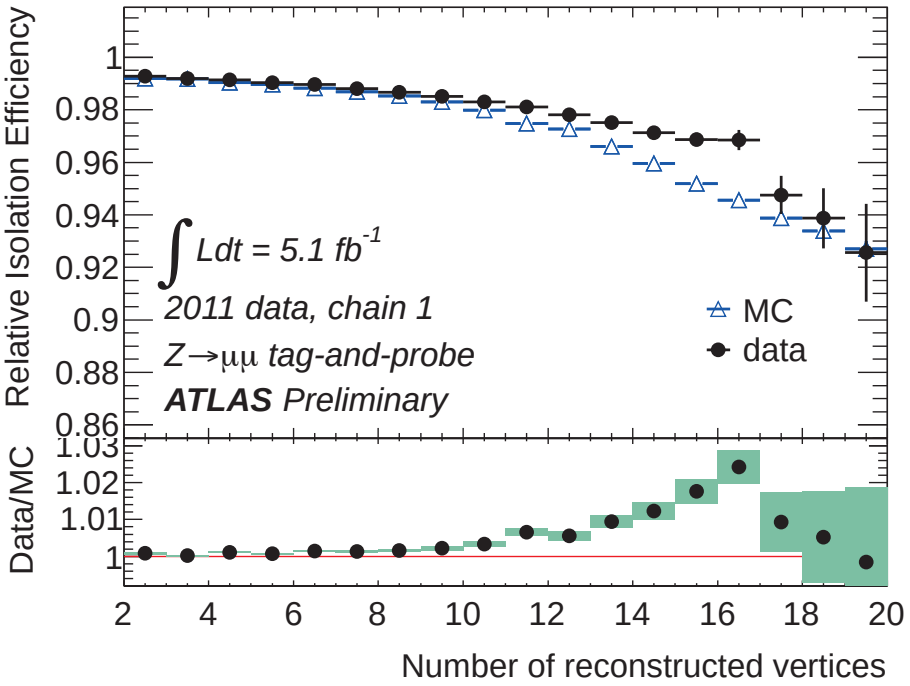


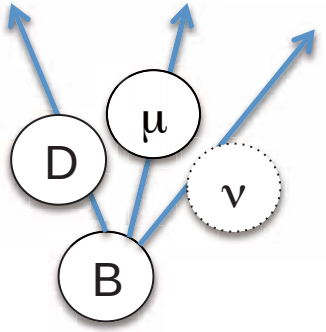


- σ_z (ビーム軸方向) ~ 50 um
- σ_x (ビーム軸垂直方向) ~ 30 um

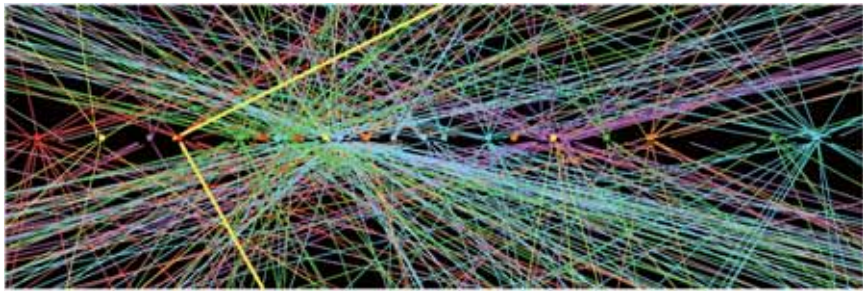
データ解析におけるパイルアップ対策

- カロリメータを用いた Isolated muon の選別



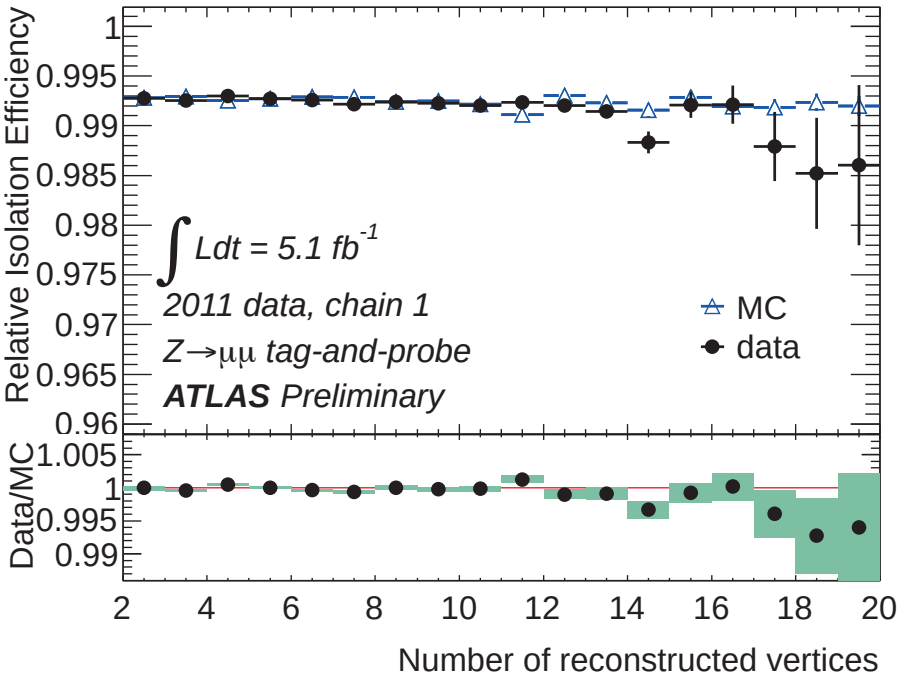


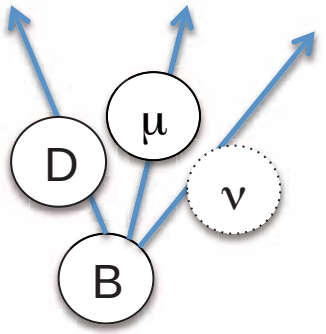
Calorimeter Based Isolation
ΣE_T ($\Delta R<0.5$)/p_T < 0.14



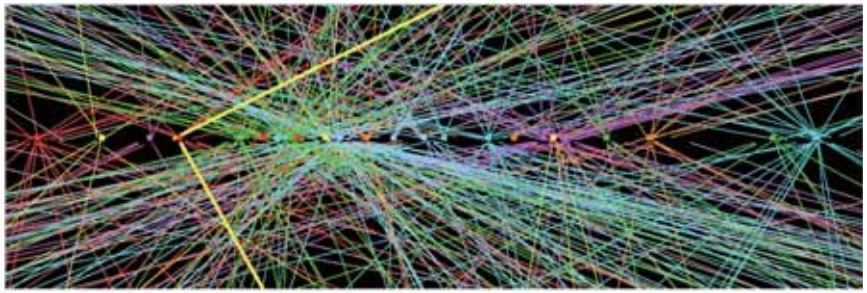
データ解析におけるパイルアップ対策

- 衝突点の情報を用いたIsolated muon の選別



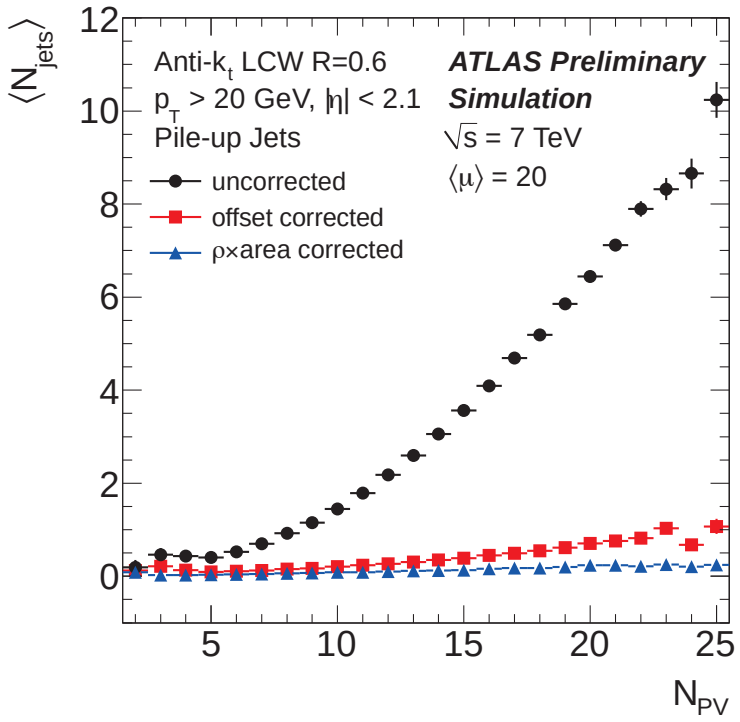


Track Based Isolation
$\Sigma p_T\ (\Delta R<0.5)/p_T < 0.15$

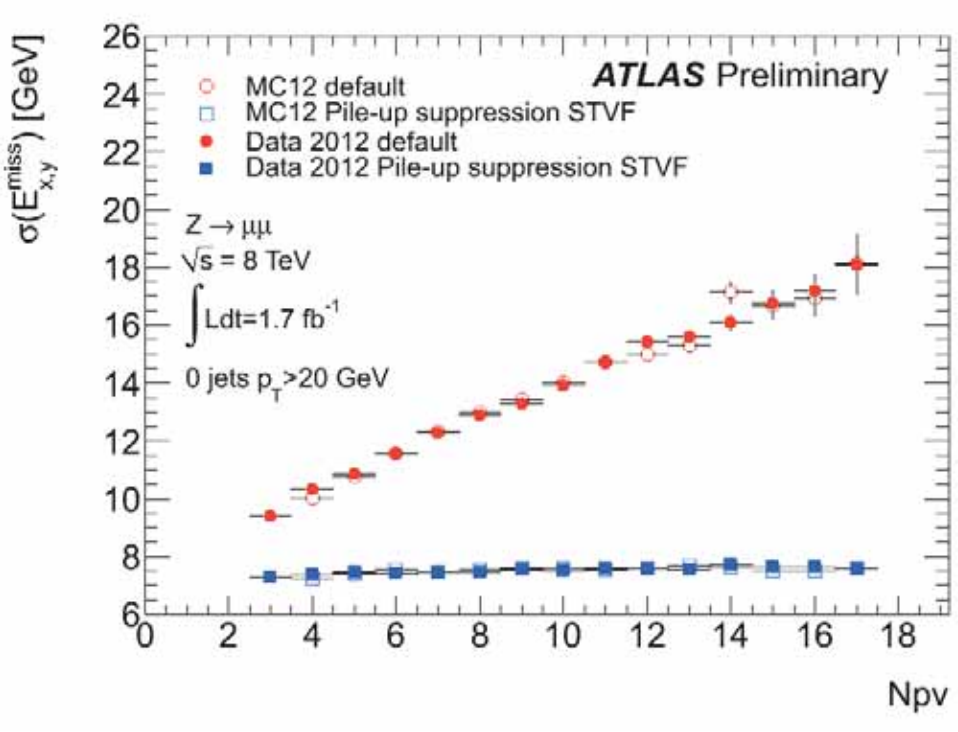


パイルアップ対策

- ハドロンカロリメータ (ジェット & Missing E_T)



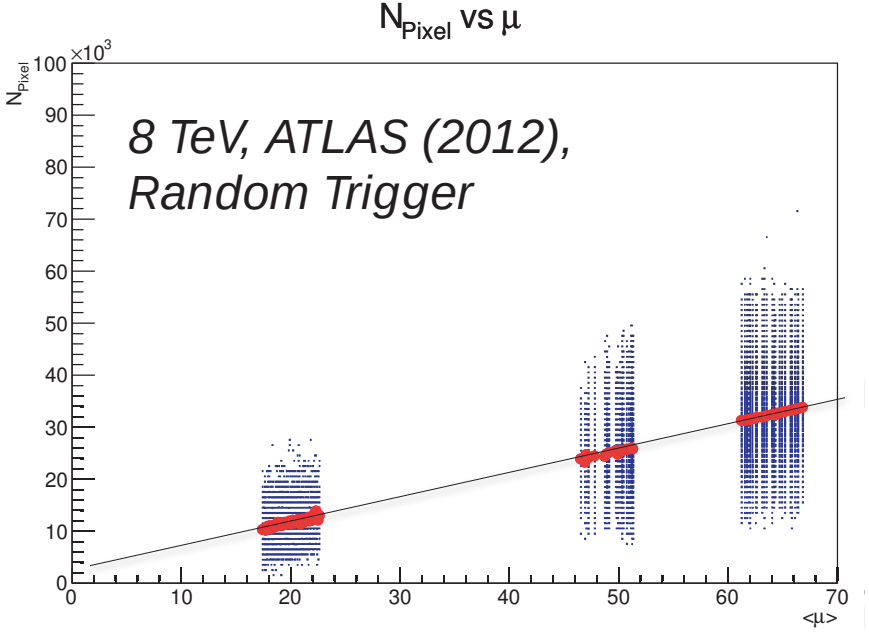
ジェット数



Missing ET 分解能

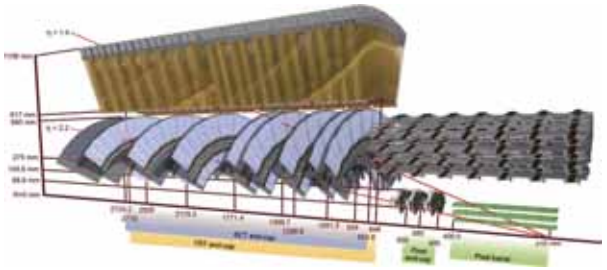
パイルアップ対策

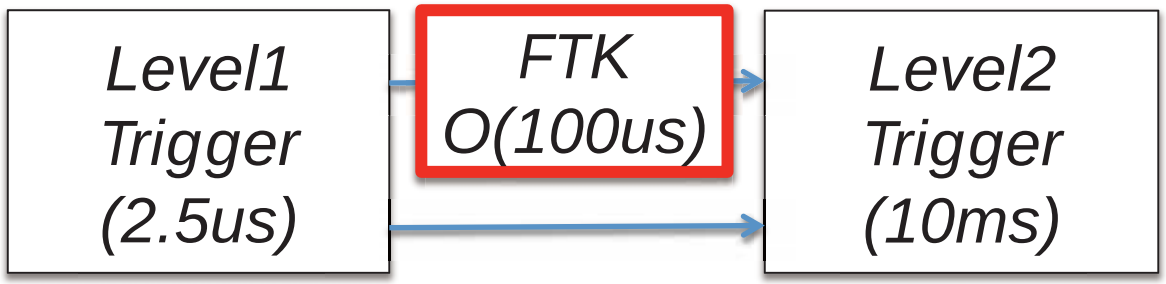
- パイルアップ対策として有効な手段
  - 再構成オブジェクトと衝突点の対応付け
  - 飛跡検出 & 衝突点再構成が必須
- オフライン解析 → トリガー
  - isolation lepton, missing ET の trigger の改善は必須
- ヒット数は線形で増加
  - 50,000 Pixel ヒット
    - Occupancy < 0.1%
  - 100,000 SCT ヒット
    - Occupancy < 2%



飛跡検出の高速化の必要性

- トリガー (=時間制限あり) への応用
  - ATLAS では L2 に用いる予定。



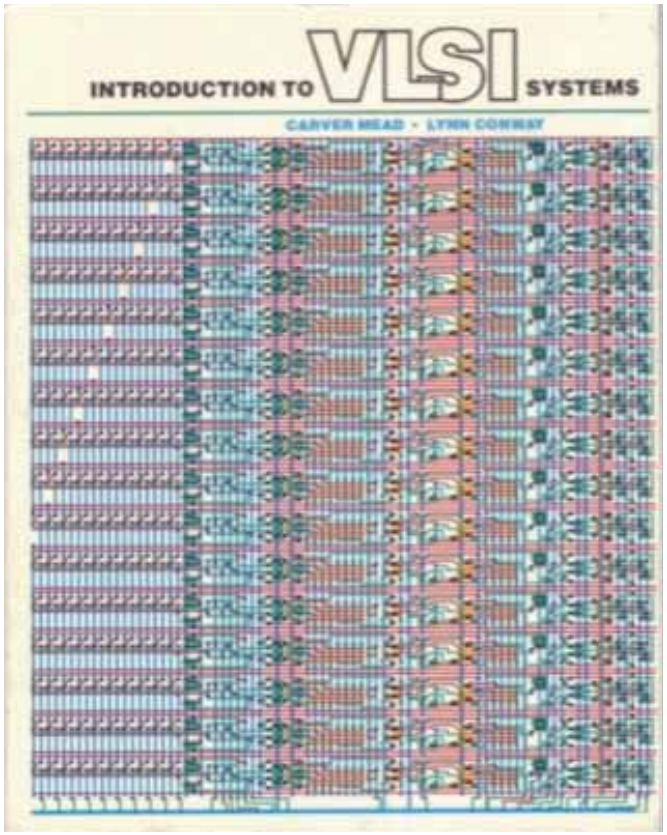


  - O(100us) での全飛跡再構成が必要
    - CPU を用いた sequential なヒット数に対し階乗でプロセス時間が増大
    - 専用の電気回路を用いた飛跡再構成システムで解決

Associative Memory を利用した “並列化” 技術

パート２
高速飛跡検出のコンセプト
Associative memory による“並列化”

Original idea in 80's



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VLSI STRUCTURES FOR TRACK FINDING

Mauro DELL'ORSO
Dipartimento di Fisica, Università di Pisa, Piazza Torricelli 2, 56100 Pisa, Italy

Luciano RISTORI
INFN Sezione di Pisa, Via Vecchia Livornese 582a, 56018 S. Piero a Grado (PI), Italy

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We discuss the architecture of a device based on the concept of *associative memory* designed to solve the track finding problem, typical of high energy physics experiments, in a time span of a few microseconds even for very high multiplicity events. This "machine" is implemented as a large array of custom VLSI chips. All the chips are equal and each of them stores a number of "patterns". All the patterns in all the chips are compared in parallel to the data coming from the detector while the detector is being read out.

1. Introduction

The quality of results from present and future high energy physics experiments depends to some extent on the implementation of fast and efficient track finding algorithms. The detection of *heavy flavor* production, for example, depends on the reconstruction of secondary vertices generated by the decay of long lived particles, which in turn requires the reconstruction of the majority of the tracks in every event.

Particularly appealing is the possibility of having detailed tracking information available at trigger level even for high multiplicity events. This information could be used to select events based on impact parameter or secondary vertices. If we could do this in a sufficiently short time we would significantly enrich the sample of events containing heavy flavors.

Typical events feature up to several tens of tracks each of them traversing a few position sensitive detector layers. Each layer detects many hits and we must correctly correlate hits belonging to the same track on different layers before we can compute the parameters of the track. This task is typically time consuming; it is usually solved using "constraint equations" which apply to hits from the same track and going through a large number of different hit combinations using a "trial and error" approach.

We propose here to use modern VLSI technology to build a device capable of solving the pattern recognition problem in a time span of a few microseconds even for the most complicated events.

2. The detector

In this discussion we will assume that our detector consists of a number of layers, each layer being segmented into a number of bins. When charged particles cross the detector they hit one bin per layer. No particular assumption is made on the shape of trajectories: they could be straight or curved. Also the detector layers need not be parallel nor flat. This abstraction is meant to represent a whole class of real detectors (drift chambers, silicon microstrip detectors etc.). In the real world the coordinate of each hit will actually be the result of some computation performed on "raw" data: it could be the center of gravity of a cluster or a charge division interpolation or a drift-time to space conversion depending on the particular class of detector we are considering. We assume that all these operations are performed upstream and that the resulting coordinates are "binned" in some way before being transmitted to our device.

3. The pattern bank

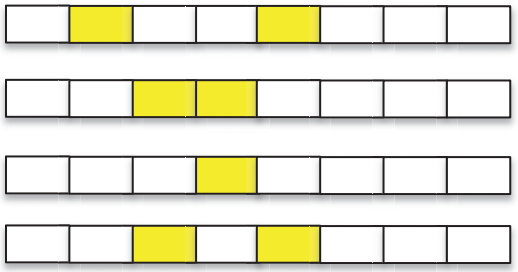
For each event we know which bins have been hit and from this information we want to reconstruct the trajectories of all the particles. We call this process *track finding*.

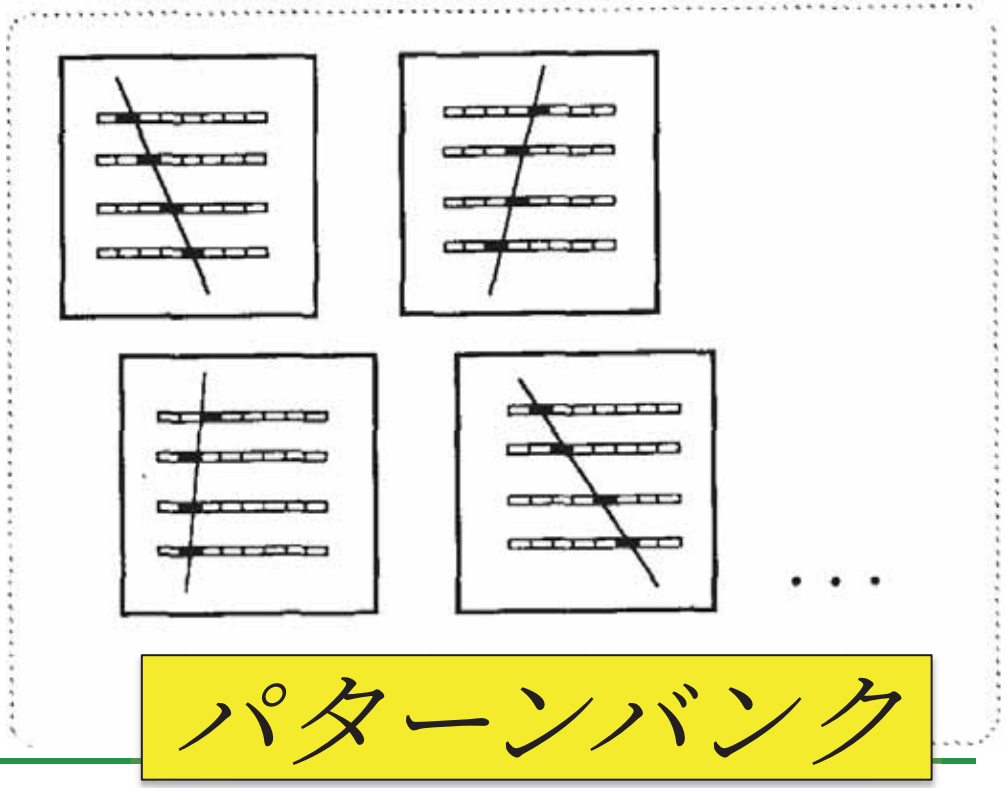
The problem of track finding can be solved, at least conceptually, by a "brute force" approach. We consider all the possible tracks that go through our detector.

We discuss the architecture of a device based on the concept of *associative memory* designed to solve the track finding problem, typical of high energy physics experiments, in a time span of a few microseconds even for very high multiplicity events. This "machine" is implemented as a large array of custom VLSI chips. All the chips are equal and each of them stores a number of "patterns". All the patterns in all the chips are compared in parallel to the data coming from the detector while the detector is being read out.

Associative Memory コンセプト

検出されたヒットパターンと、予想される全トラックパターン (データベース) を比較し、一致したパターンを “検出” されたトラックとして扱う





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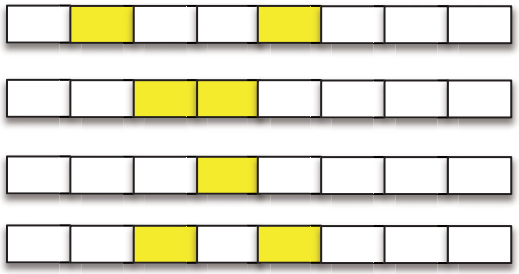
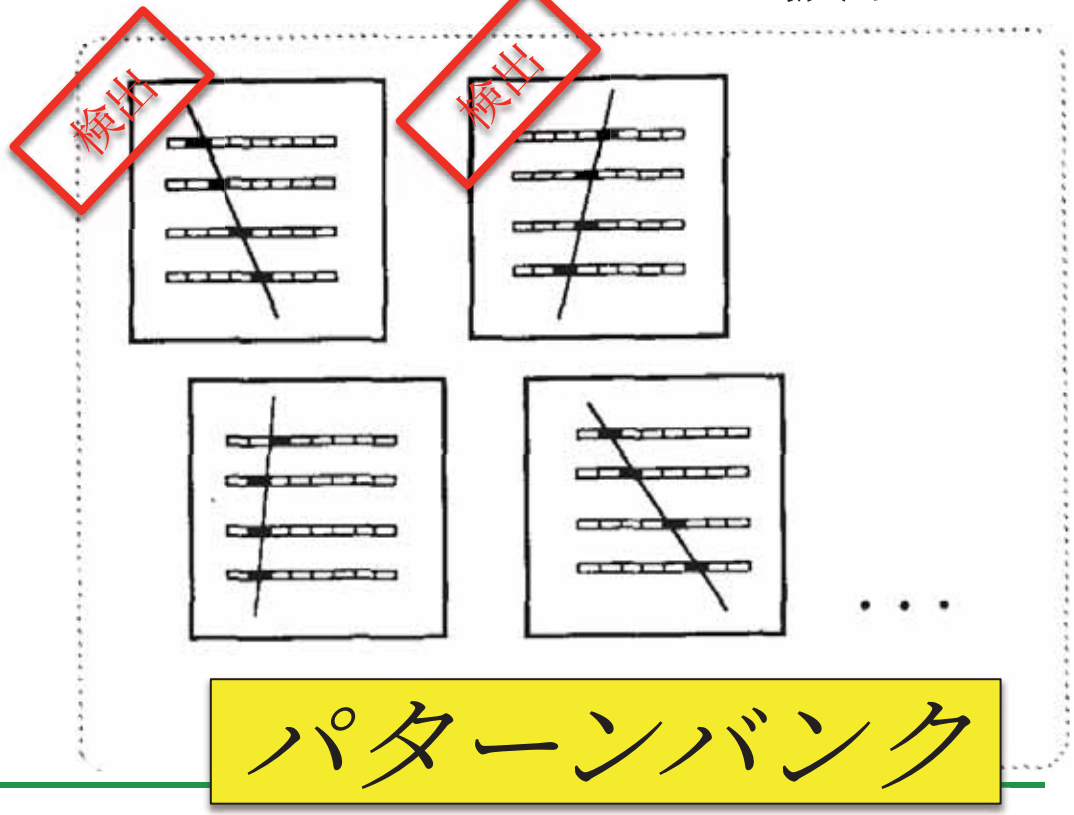
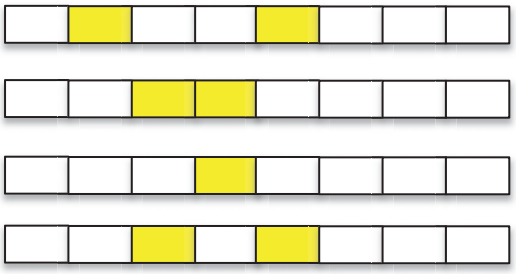




コンセプト

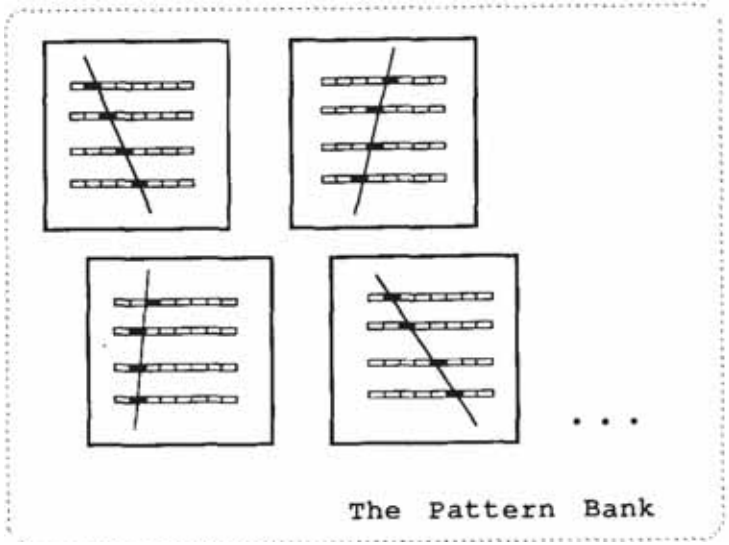
デザインにおける仮定

- ✓ 検出器は複数層からなっており、
- ✓ 各層は複数のチャンネルからなる
- ✓ 荷電粒子の通過位置をヒットによって識別
- ✓ 衝突点の制限、運動量の下限値の設定によりパターン数は有限

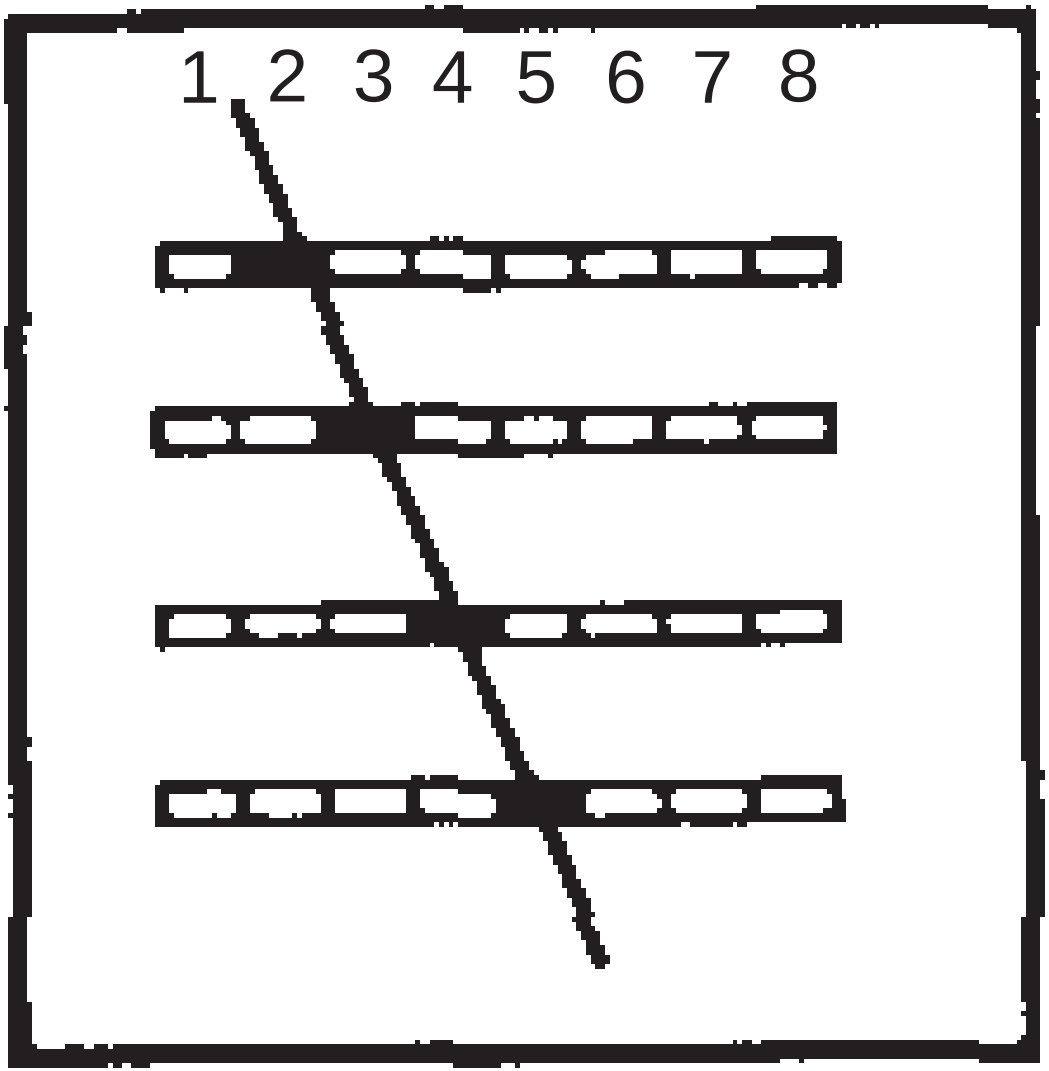


シリコン検出器

コライダー実験
(high P_T の物理)



Track Pattern “Bank”



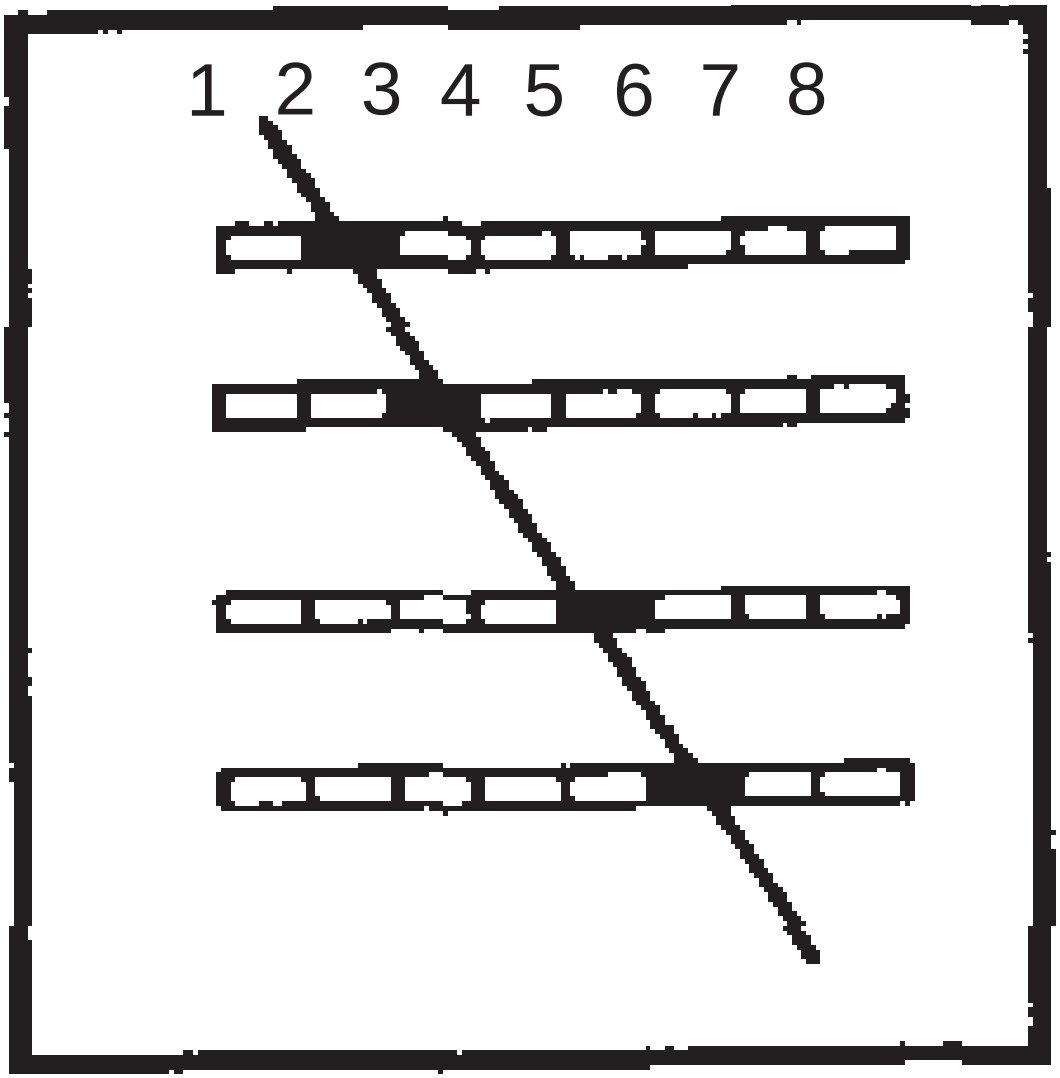
2 @ Layer3

3 @ Layer3

4 @ Layer2

5 @ Layer1

Track Pattern “Bank”



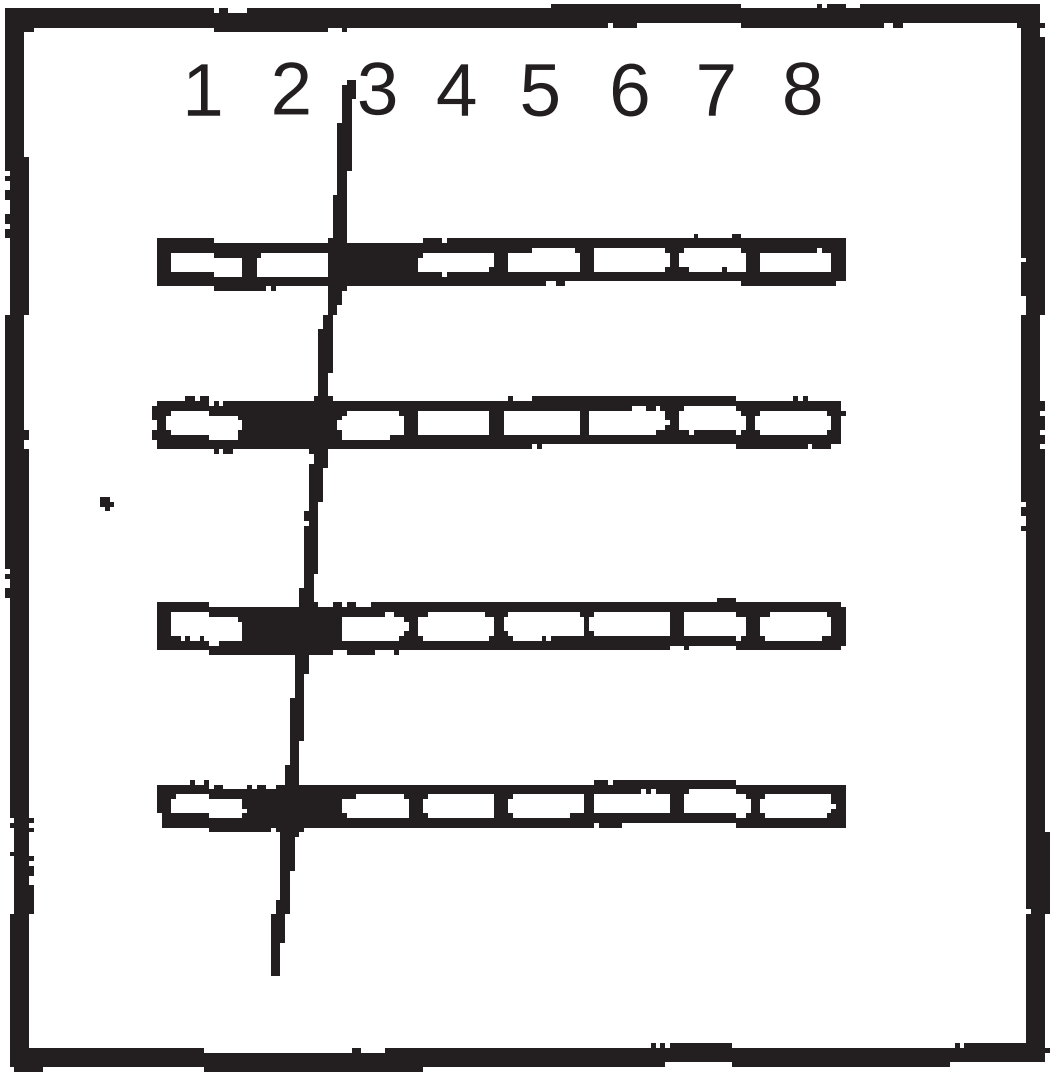
2 @ Layer3

3 @ Layer3

5 @ Layer2

6 @ Layer1

Track Pattern “Bank”



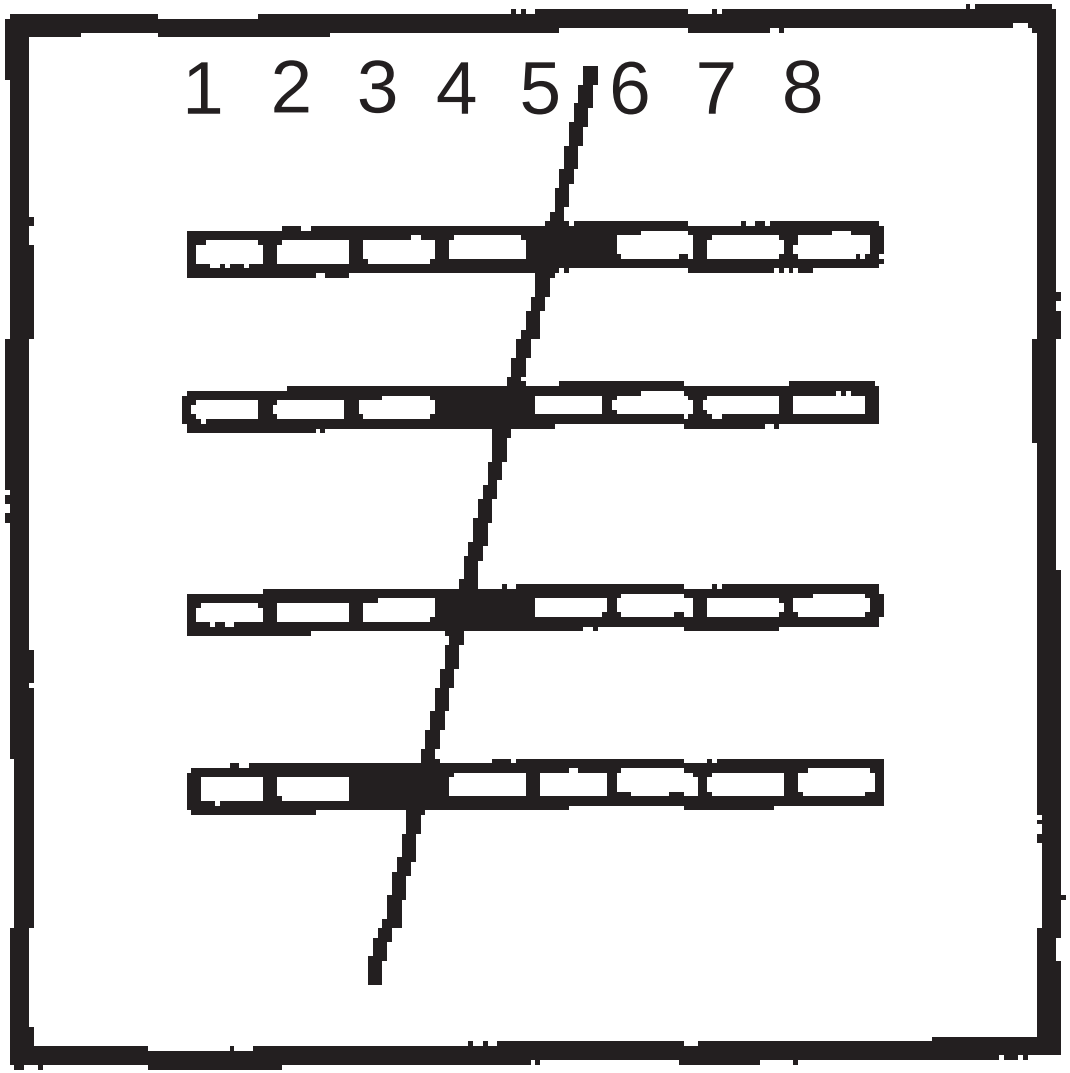
3 @ Layer3

2 @ Layer3

2 @ Layer2

2 @ Layer1

Track Pattern “Bank”



5 @ Layer3

4 @ Layer3

4 @ Layer2

3 @ Layer1

Associative Memory

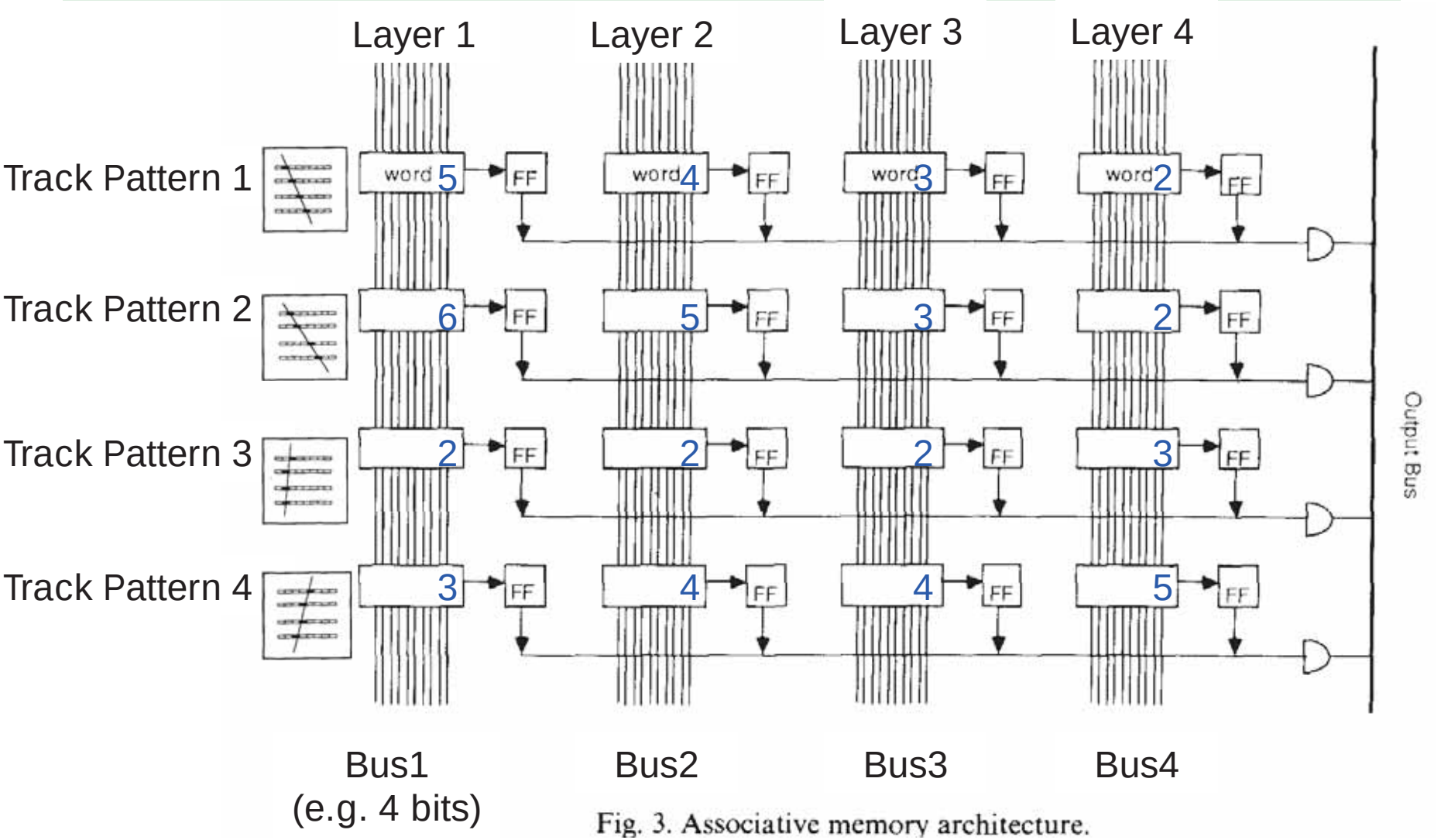
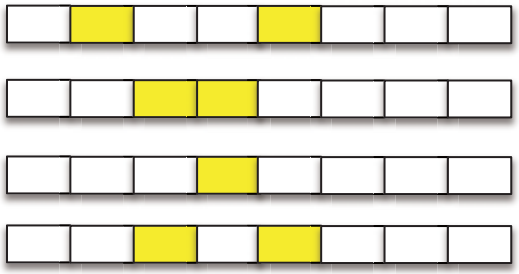
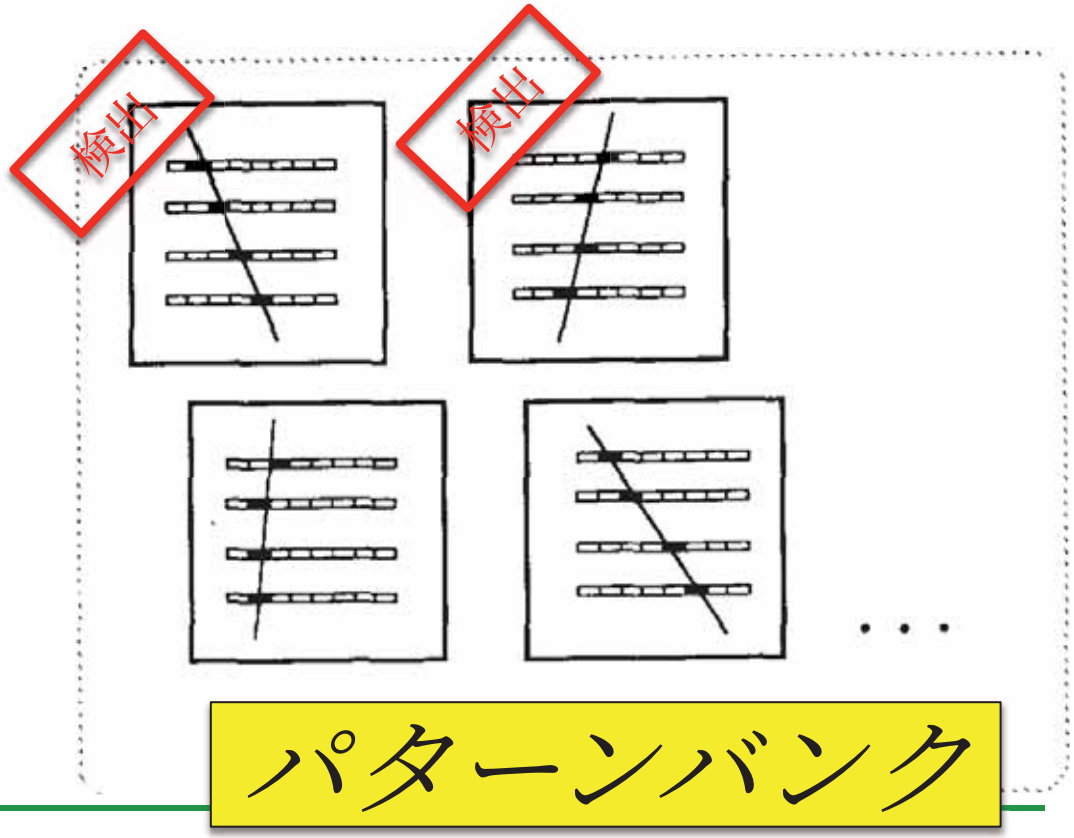


Fig. 3. Associative memory architecture.

AM メモリ動作

ヒット情報を AM メモリにロードして、
対応するトラックパターンを見つけ出す





Associative Memory

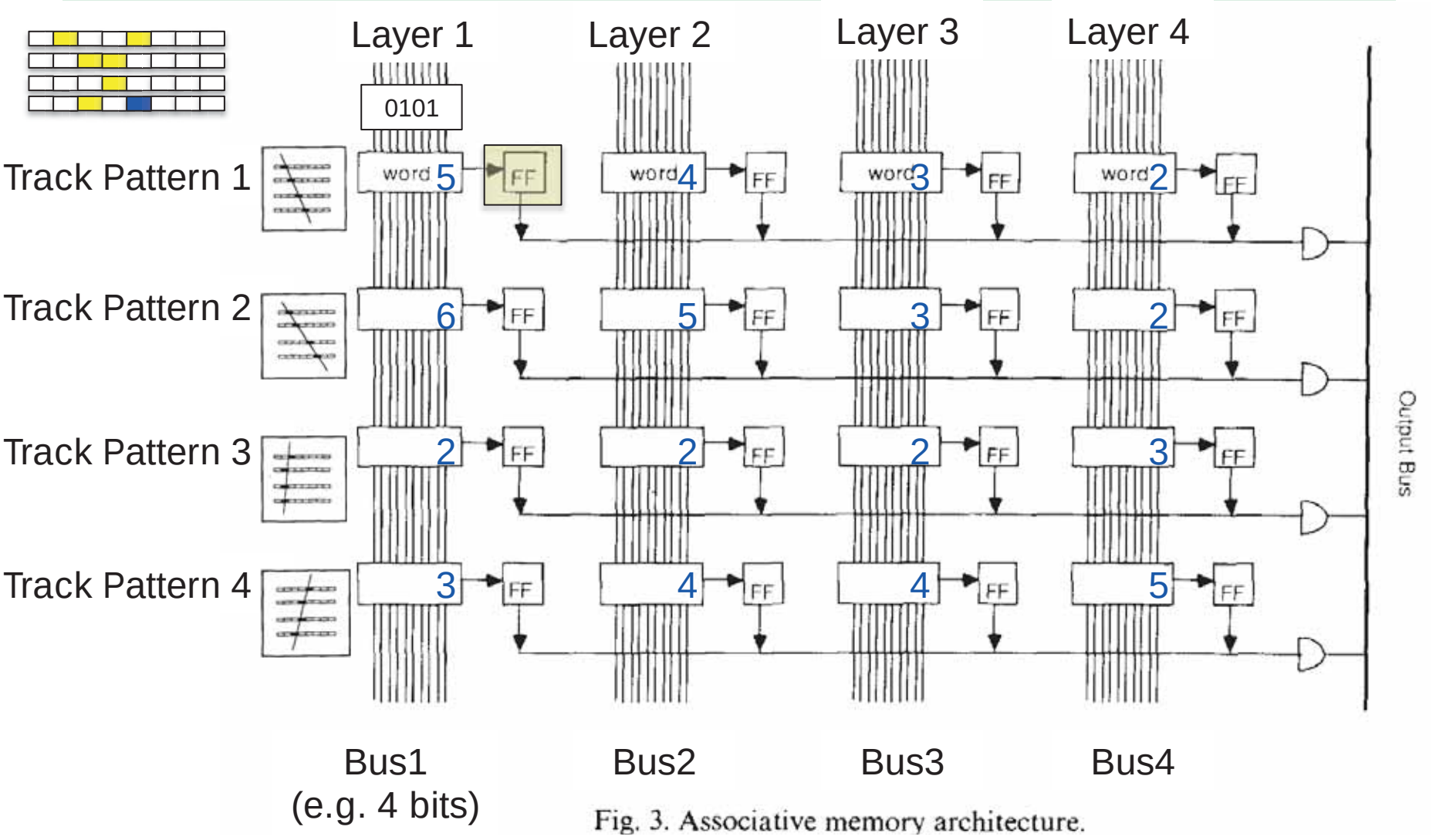


Fig. 3. Associative memory architecture.

Associative Memory

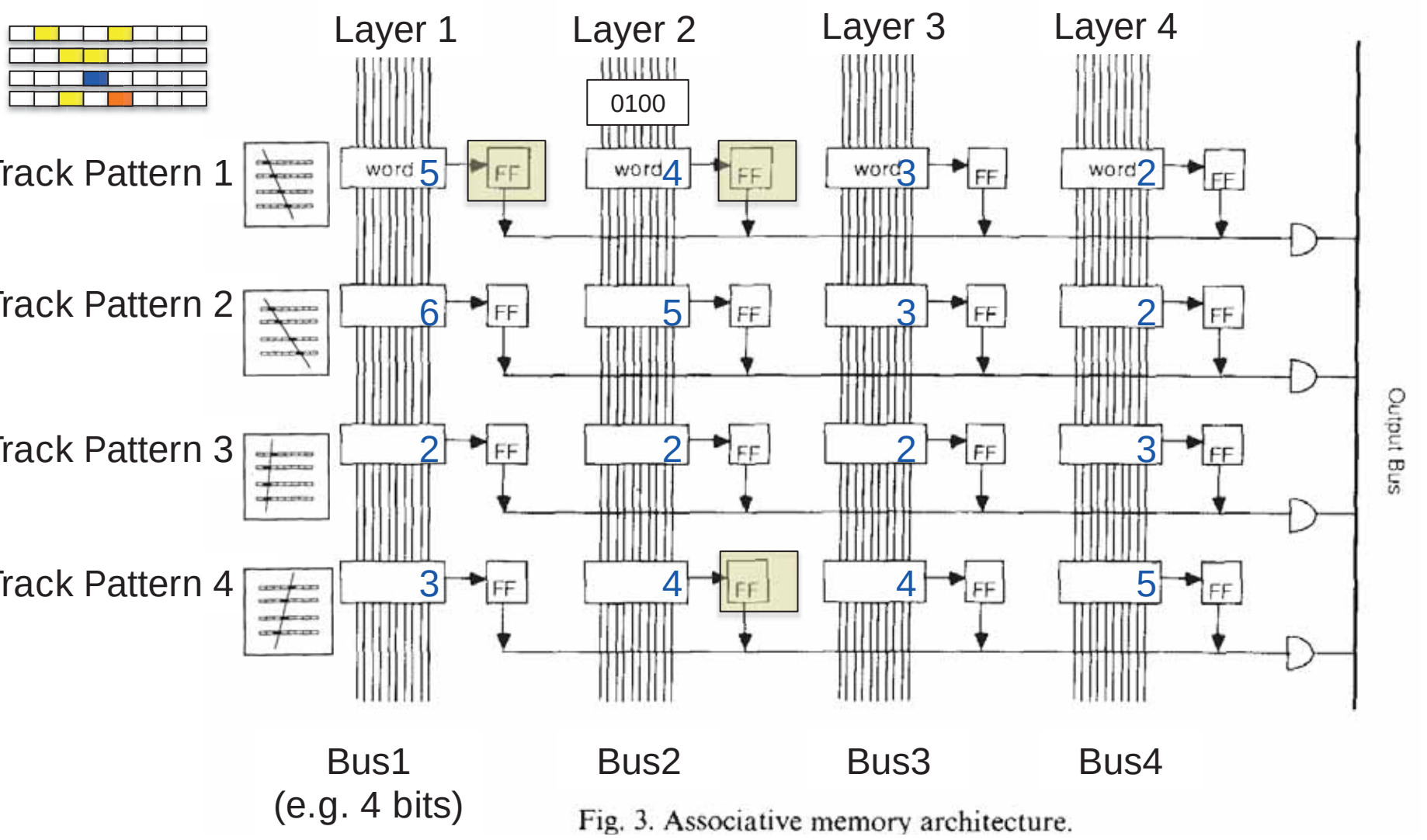


Fig. 3. Associative memory architecture.

Associative Memory

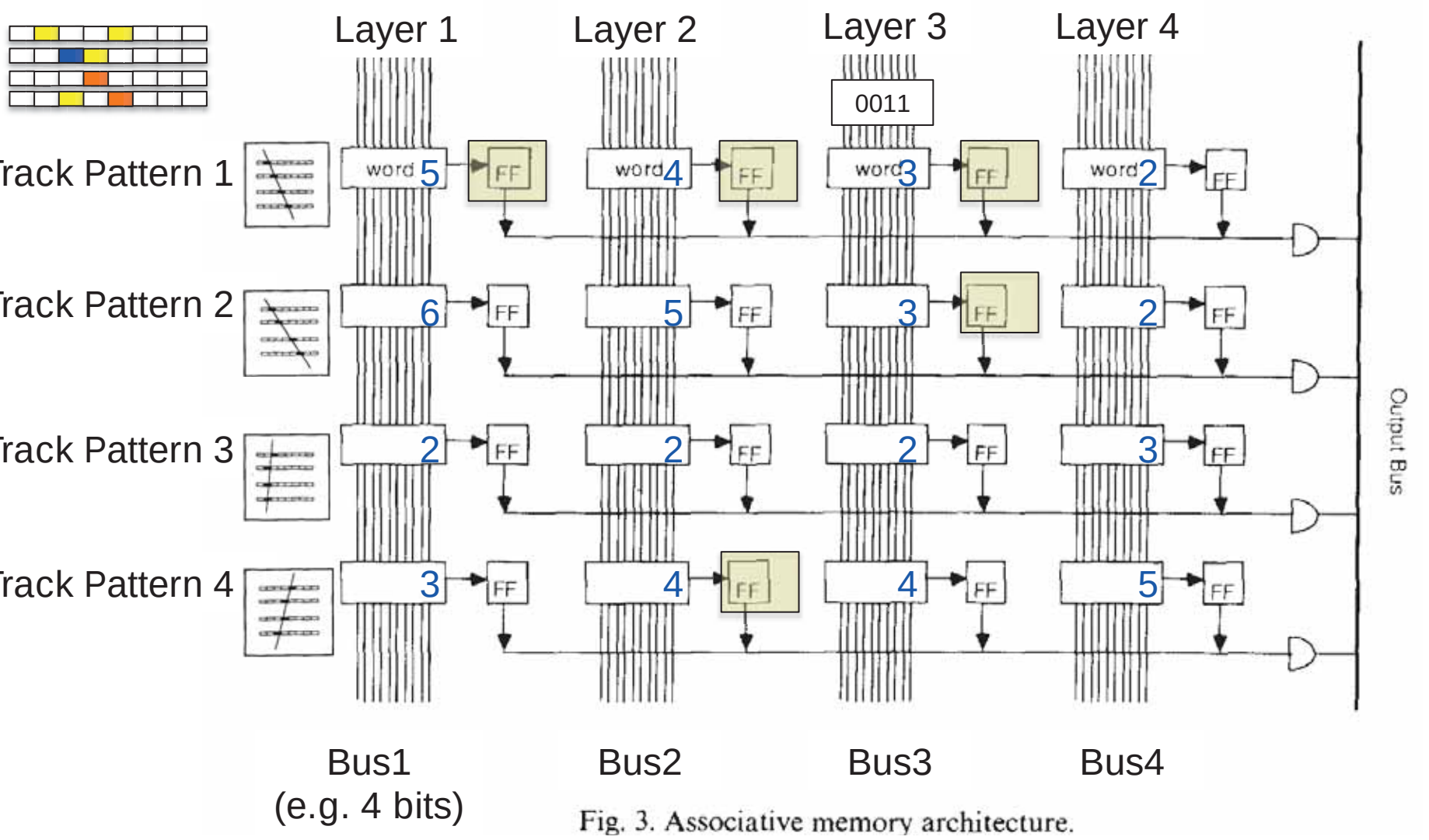


Fig. 3. Associative memory architecture.

Associative Memory

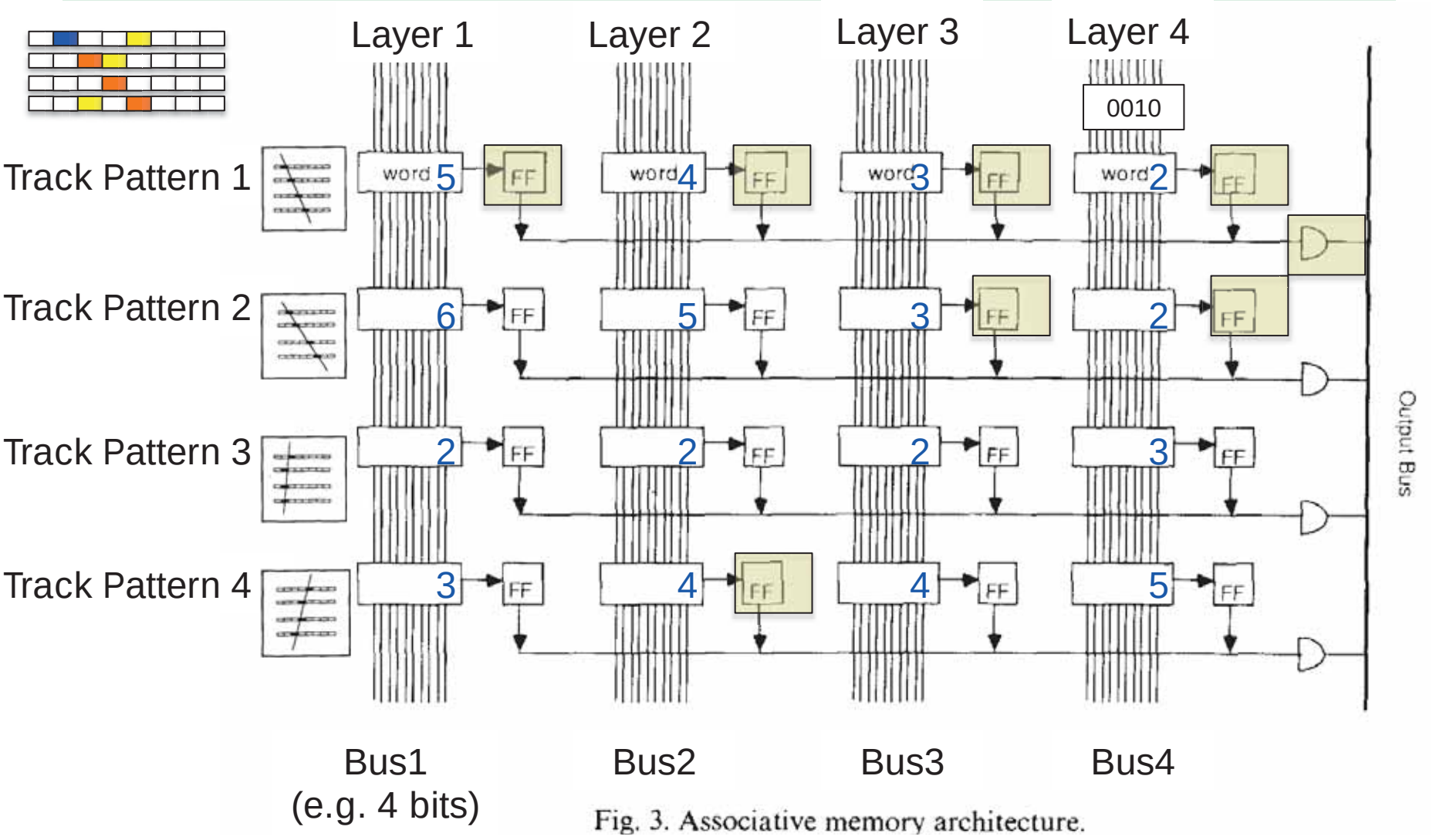


Fig. 3. Associative memory architecture.

Associative Memory

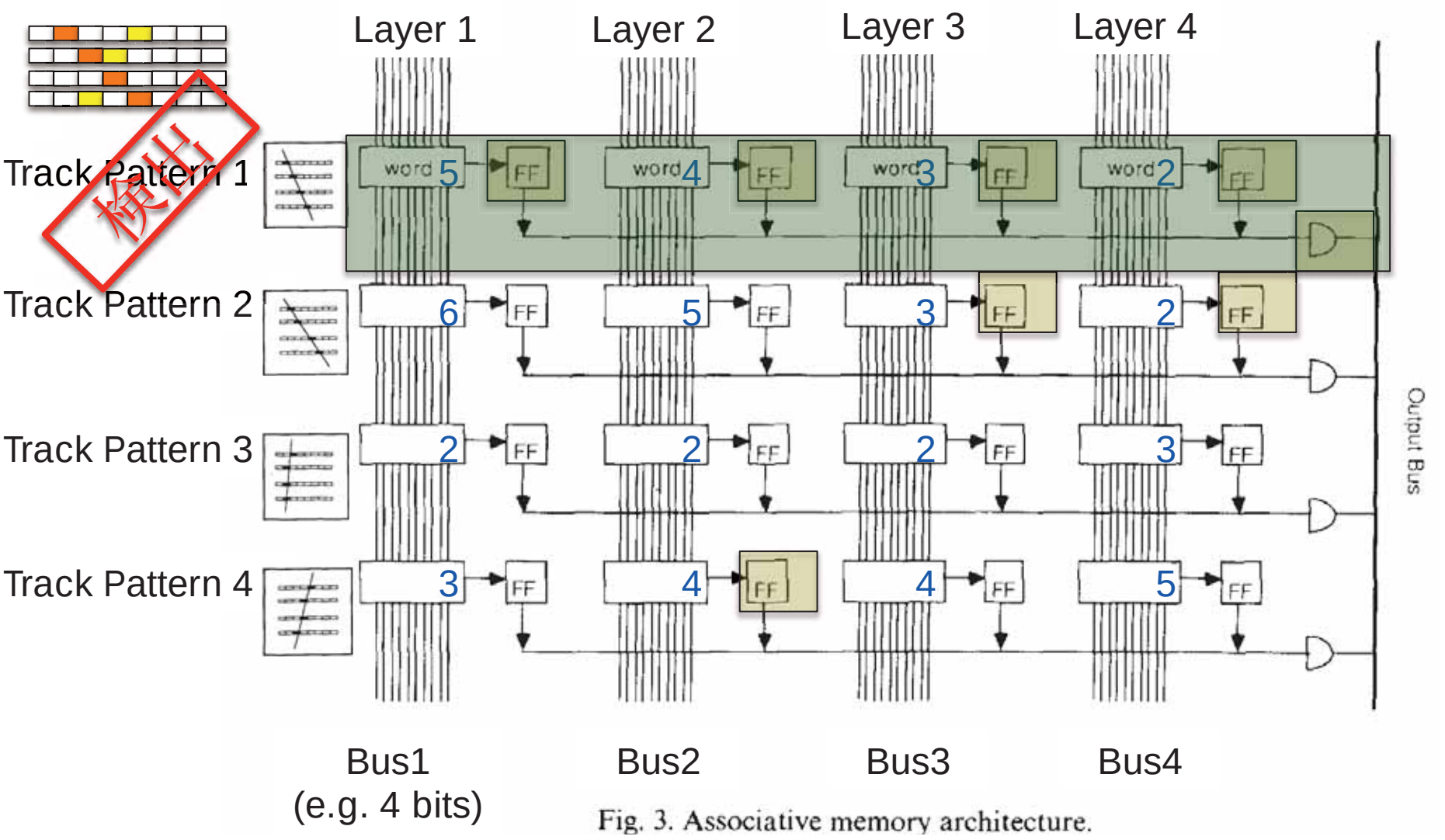


Fig. 3. Associative memory architecture.

Associative Memory

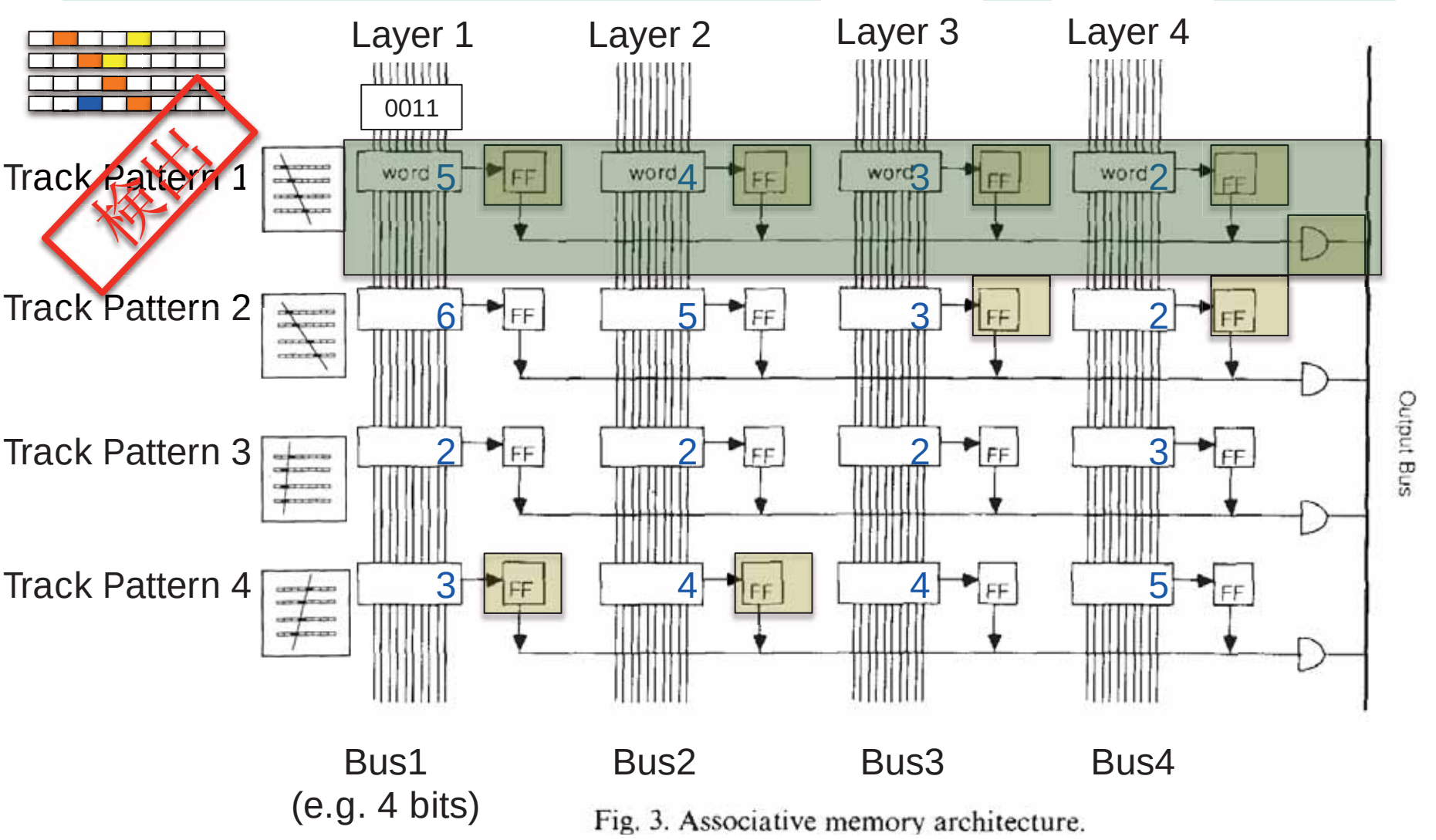


Fig. 3. Associative memory architecture.

Associative Memory

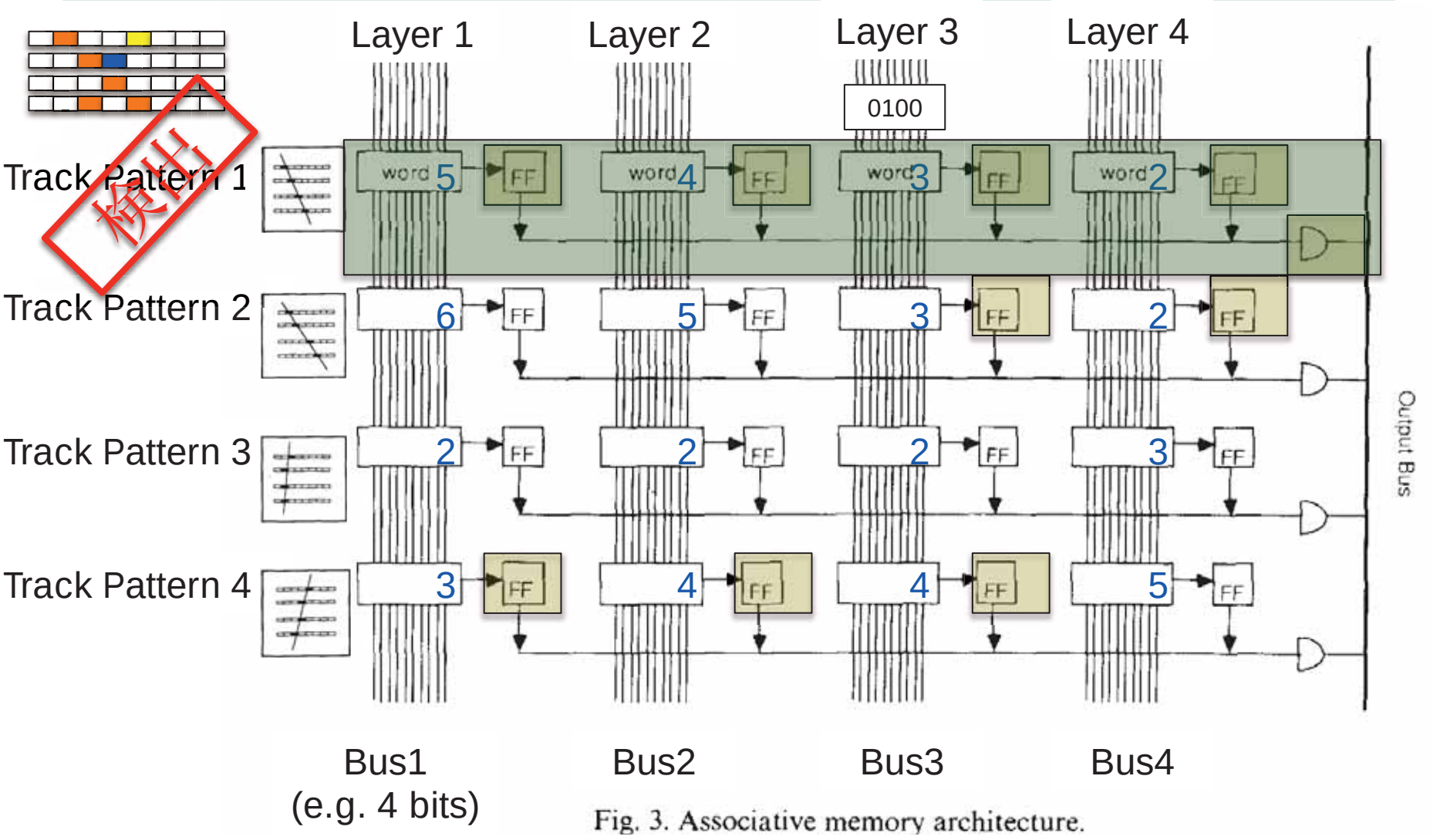


Fig. 3. Associative memory architecture.

Associative Memory

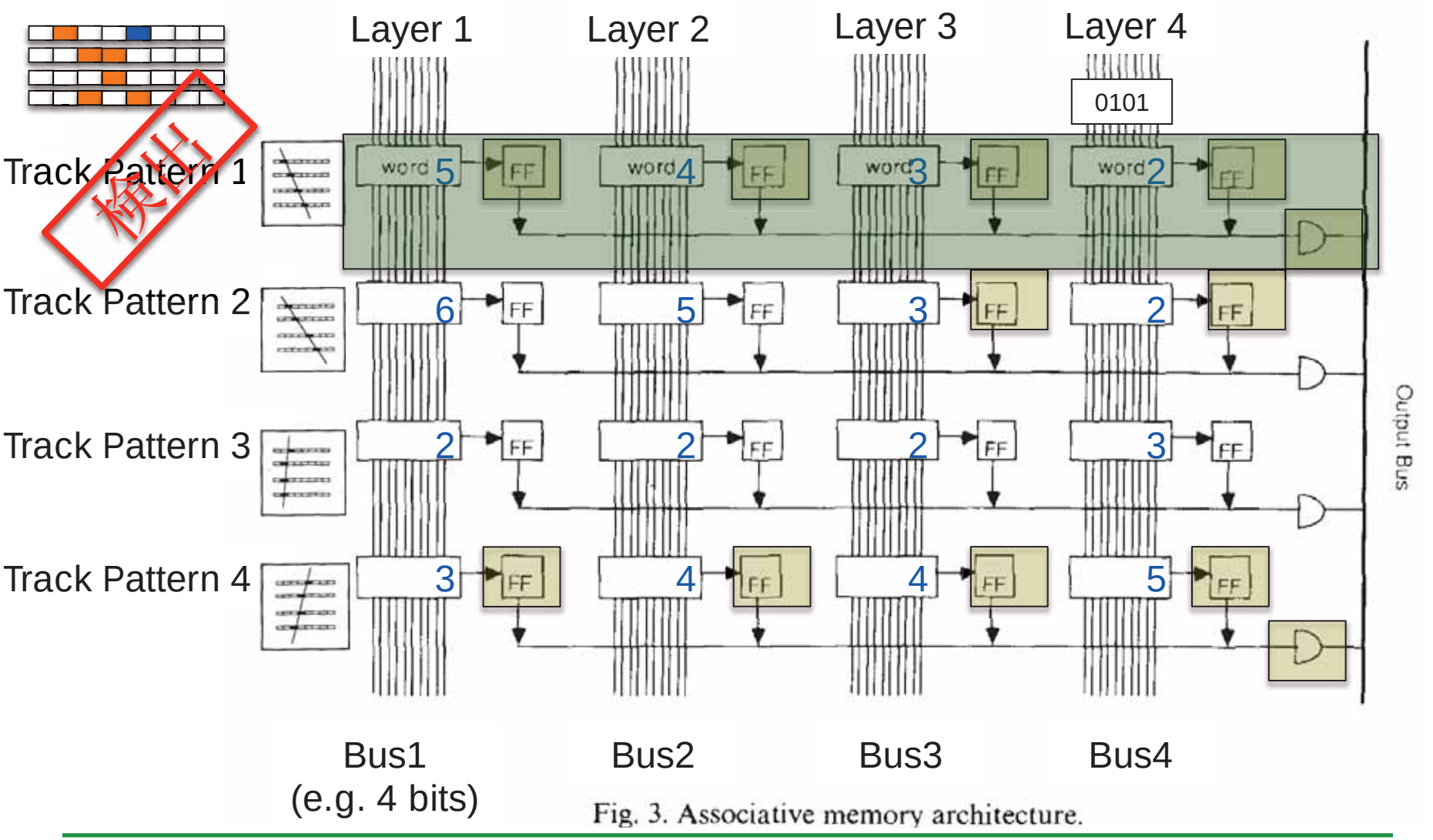


Fig. 3. Associative memory architecture.

Associative Memory

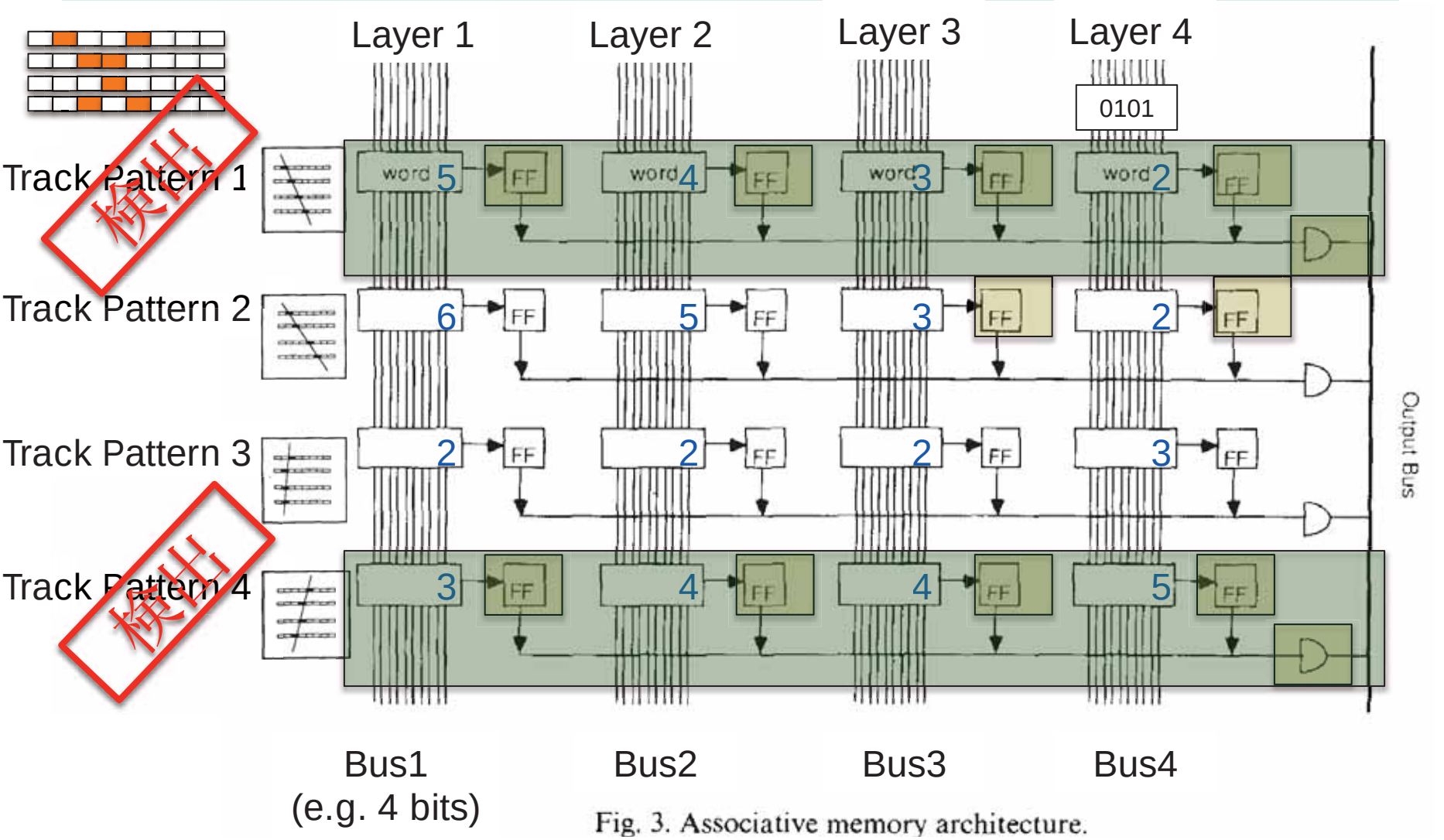


Fig. 3. Associative memory architecture.

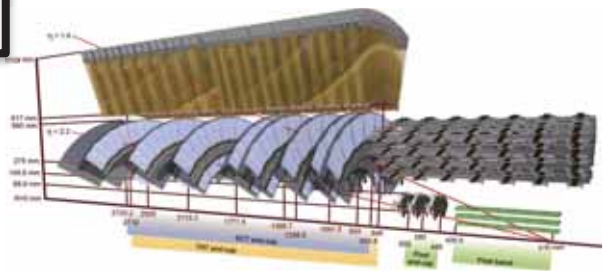
AM を用いたアプローチの特徴

- 全てのパターンと同時に比較
- プロセス時間はヒット数に比例
  - 全ヒットをロードし次第
    全パターン認識は完了
  - 階乗で増えることはない (制御可能)

- パターンバンクに保存することができる、
  トラックパターン数によって性能が決定
  - AM メモリの高集積化がポイント
  - 飛跡検出の効率

ATLAS FastTracker Processor

86 M ch



Detector (Pixel & SCT)
(Selected by Level 1 Trigger)

Data Re-formatting

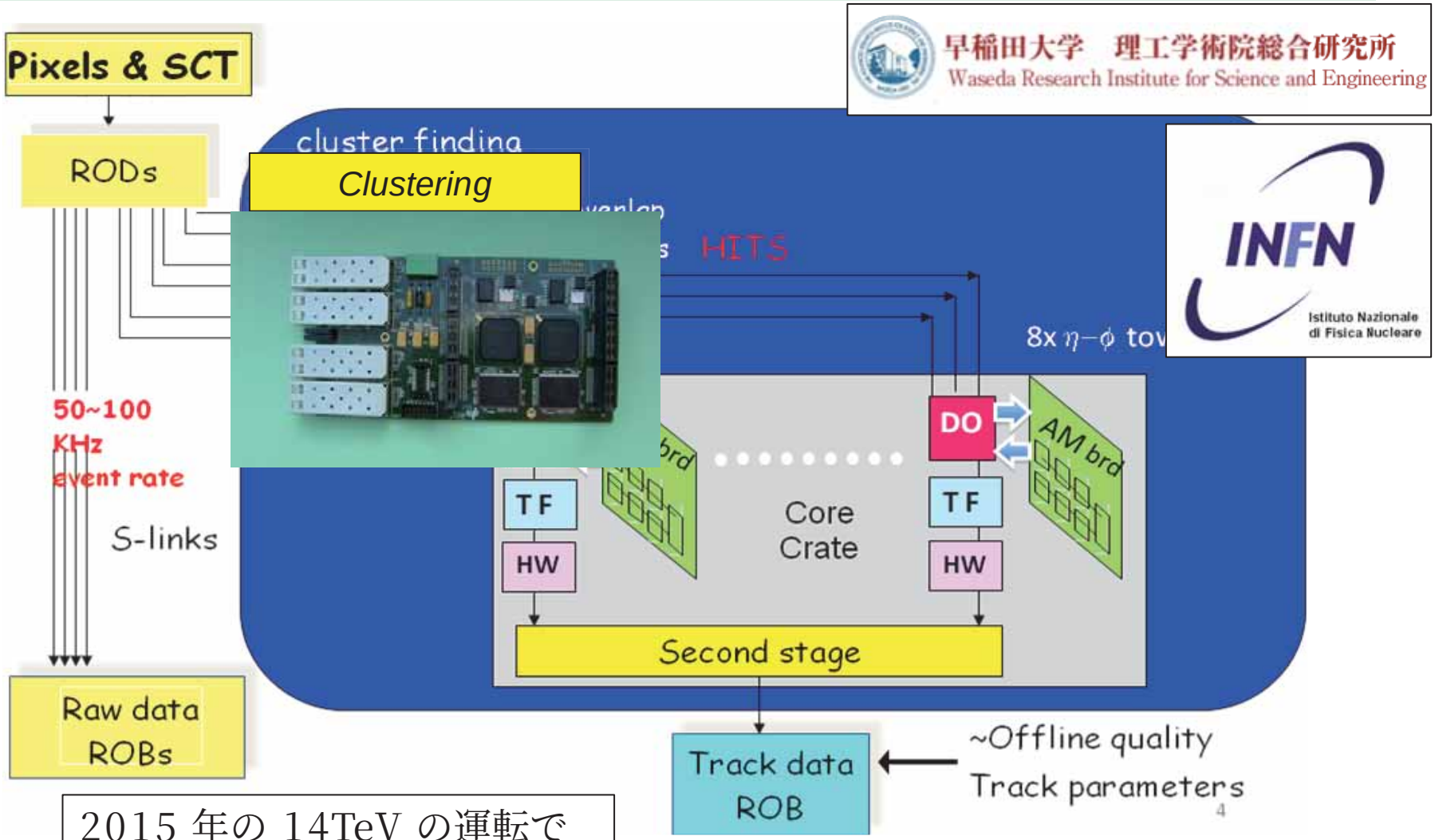
Track finding (AM chip) | Track finding (AM chip) | … | Track finding (AM chip)

Track fitting | Track fitting | Track fitting

Send the track list out to Level-2 trigger system

(η, ϕ) で検出器を 64 領域 (Tower) に分割し、更なる “並列処理”
100 micro second 程度での全飛跡再構成を完了し、L2 を改善

ATLAS FastTracker Processors

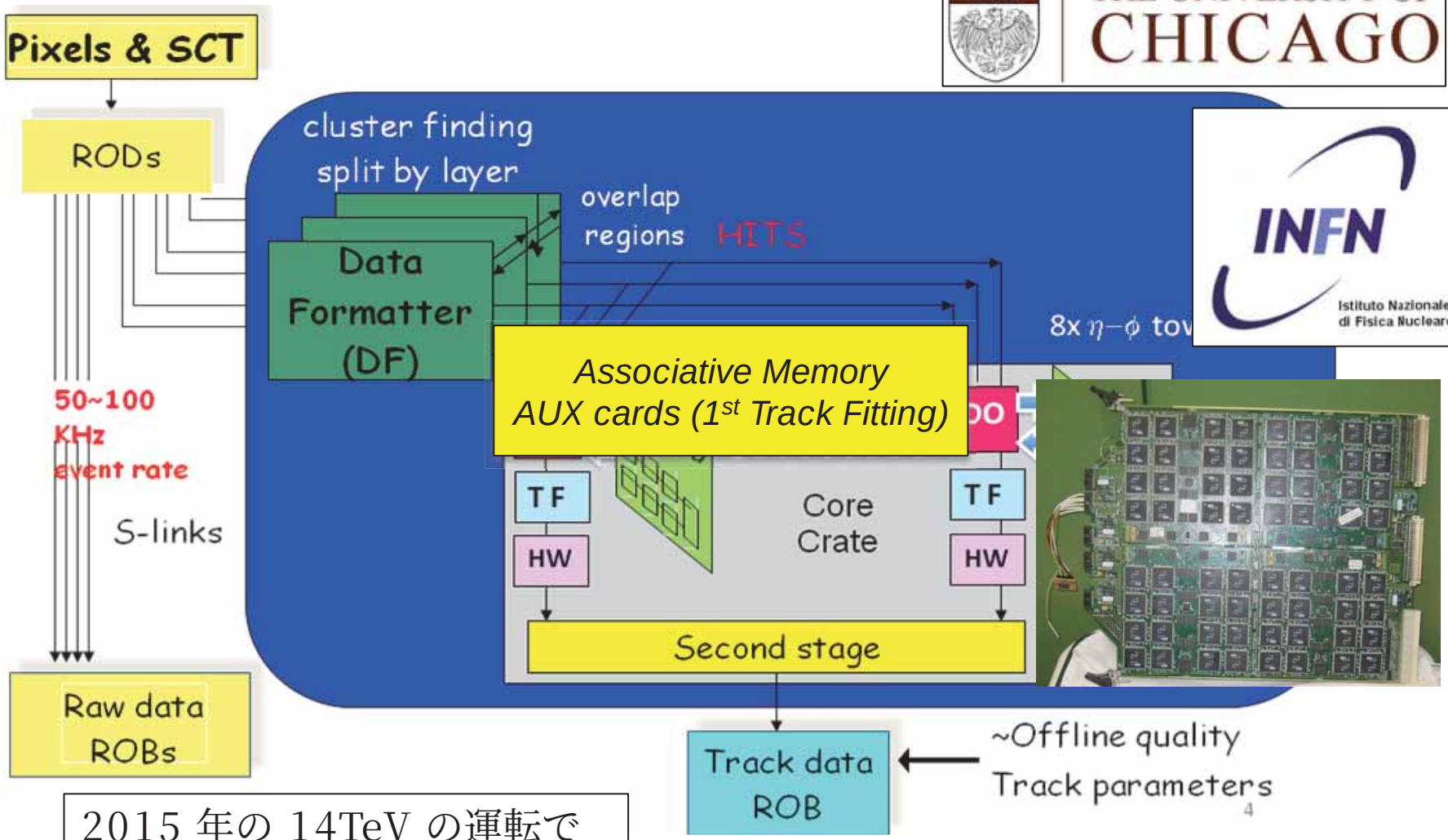


2015 年の 14TeV の運転で運転 (試験) 開始予定

ATLAS FastTracker Processors

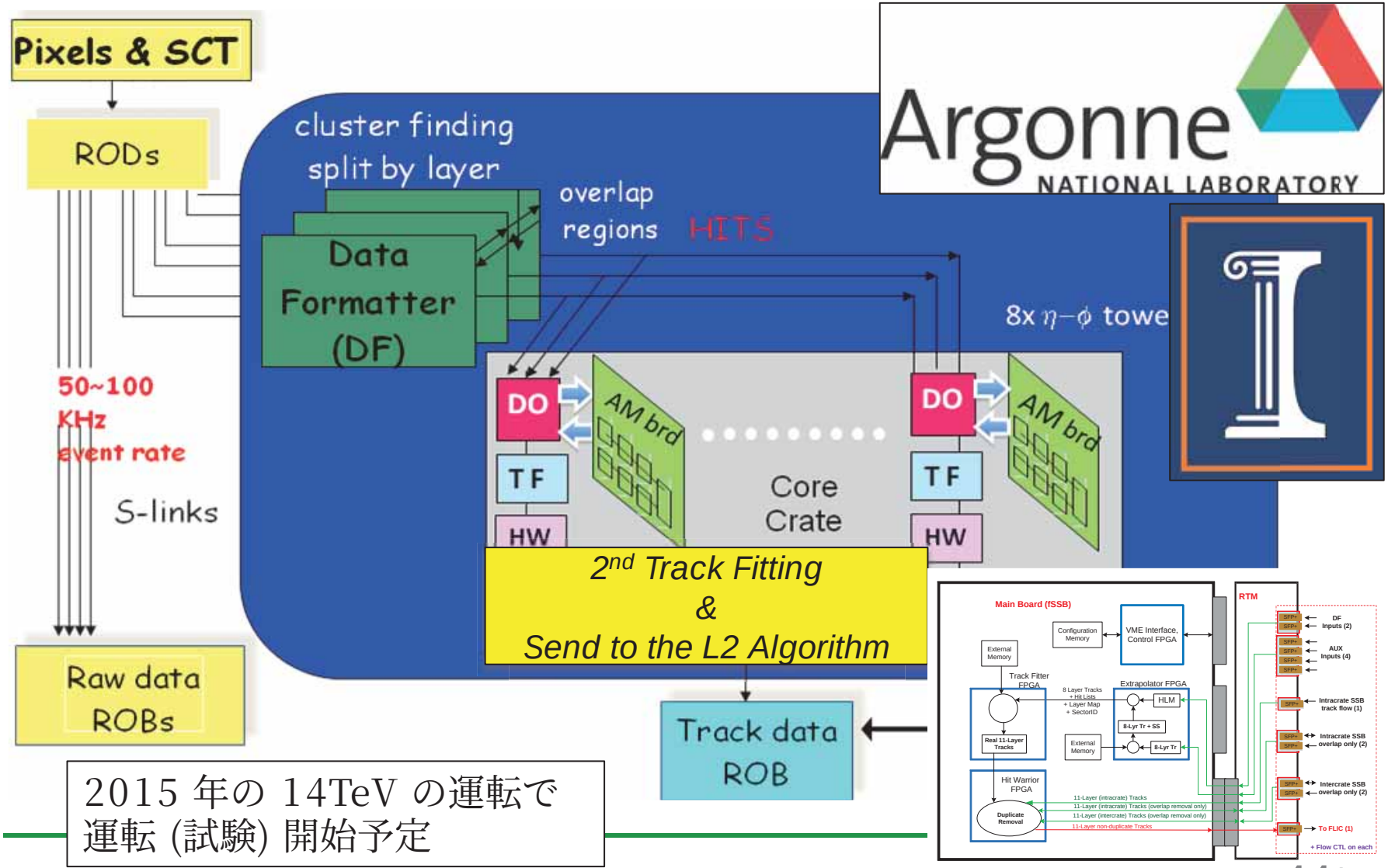
2015 年の 14TeV の運転で運転 (試験) 開始予定

ATLAS FastTracker Processors



2015 年の 14TeV の運転で
運転 (試験) 開始予定

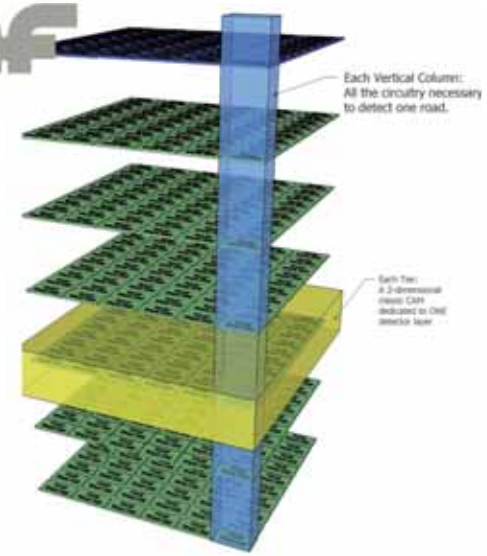
ATLAS FastTracker Processors



2015 年の 14TeV の運転で
運転 (試験) 開始予定

将来研究

- *Data Formatting ATCA backplane system*
  - ATLAS で使用予定 & 将来研究
- *Associative Memory with 3D CAM*
  - 将来研究
- *Track Fitting with Graphical Processing Unit*
  - 将来研究

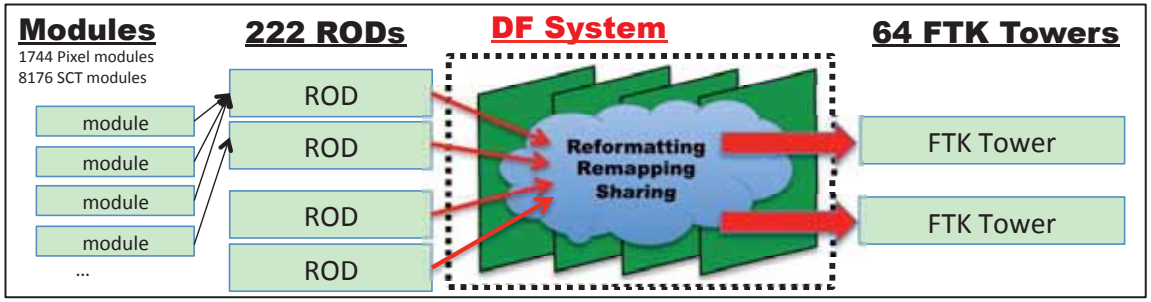


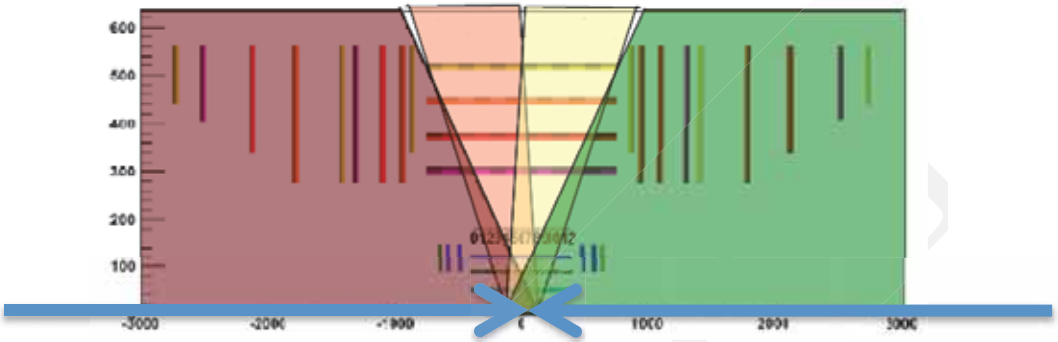
パート３
最近の技術開発の紹介

Data Formatter System (ATCA backplane system)

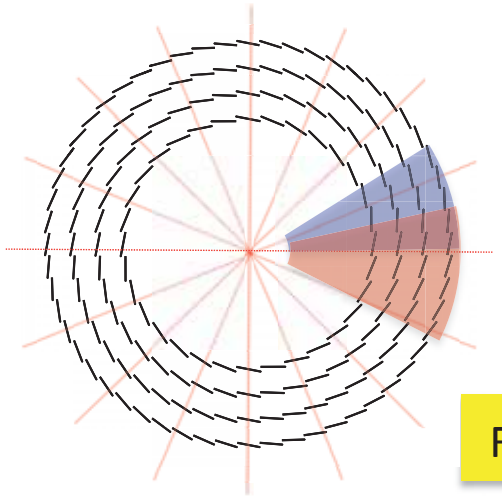
Data Formatting

- *処理系の "並列化" のための準備*
  - Tower 構造にあわせデータを再構築 (150k hits / event)
  - Inefficiency を防ぐための Tower 間のデータ共有





For η (4)

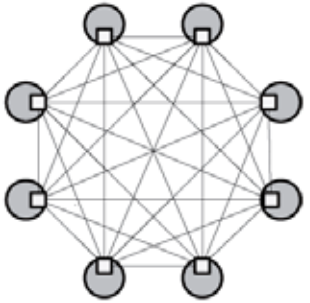


For ϕ (16)

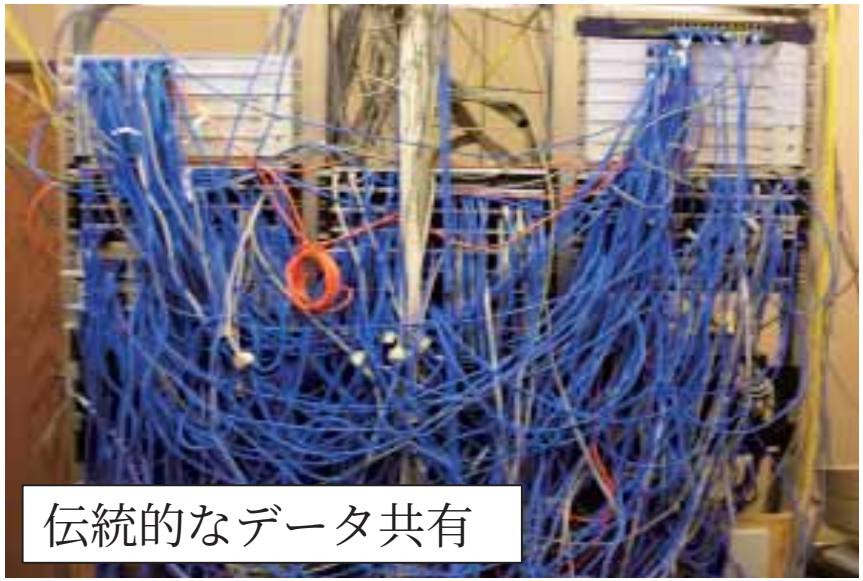
システム内部での高速のデータ通信

ATCA システムを適用

Advanced Telecommunication Computing Architecture (ATCA)



- Backplane が任意のボードのペアの シリアル通信 (up to 10 Gb/s) を独立にサポート
  - 参考 VME: パラレルバス (D/A) を全ボードが共有
- クレート全体で一枚のボードの用に取り扱える

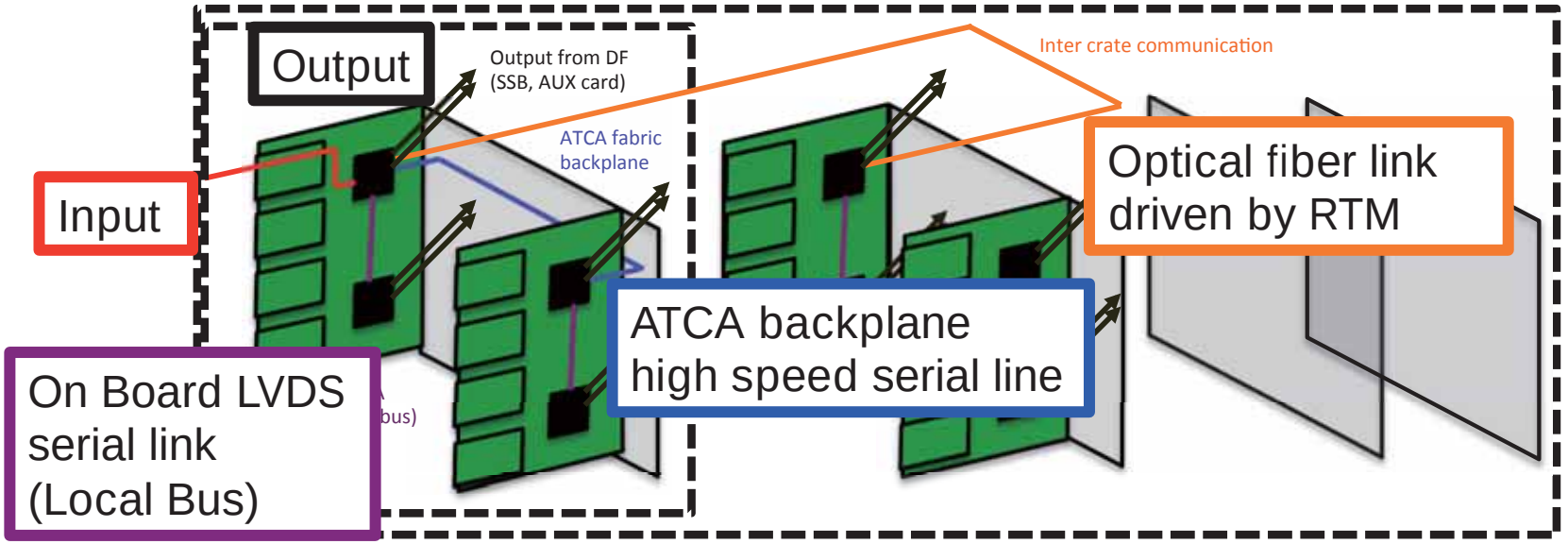


伝統的なデータ共有

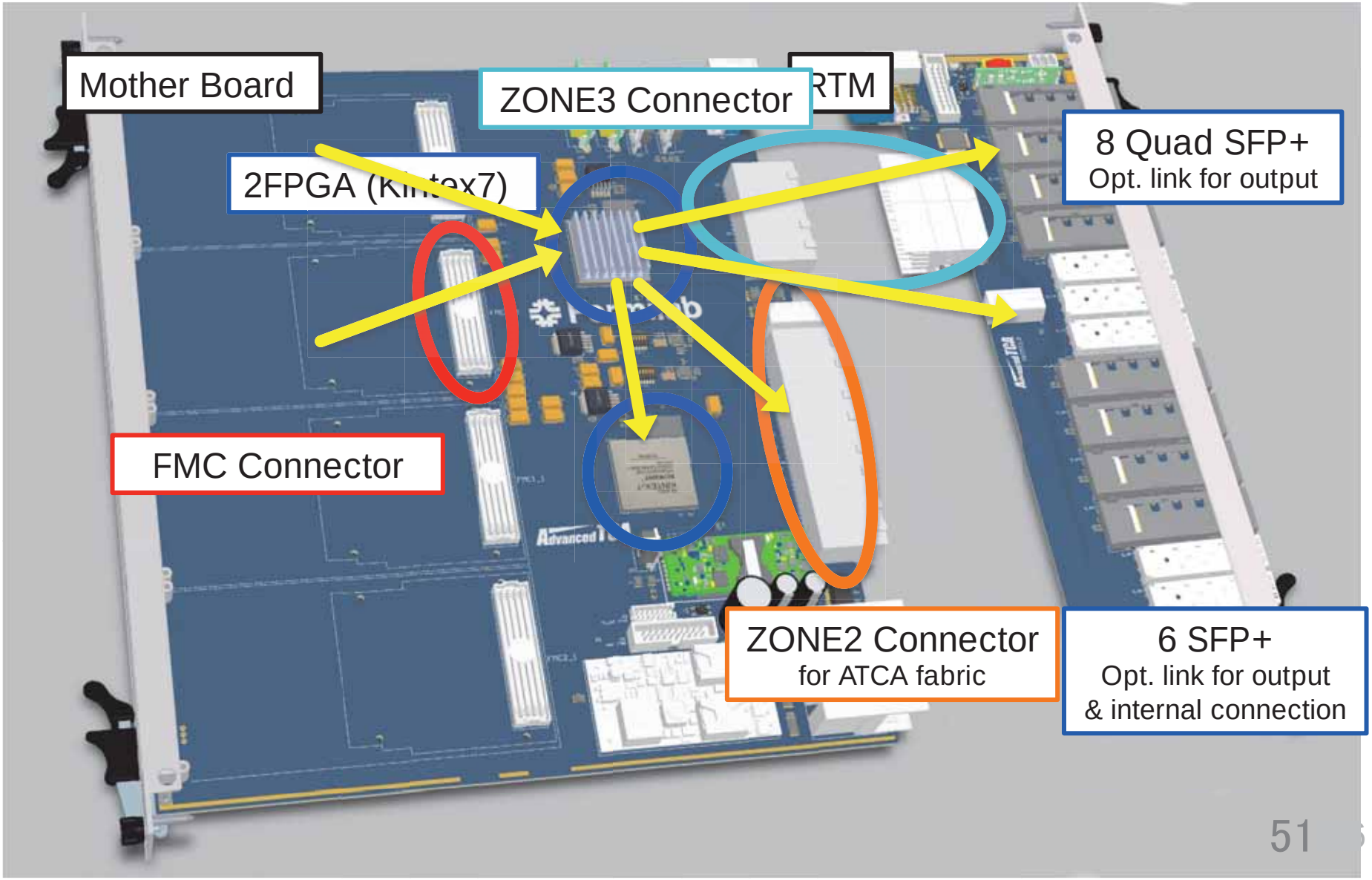
ATCA を用いたデータ共有

システム概観

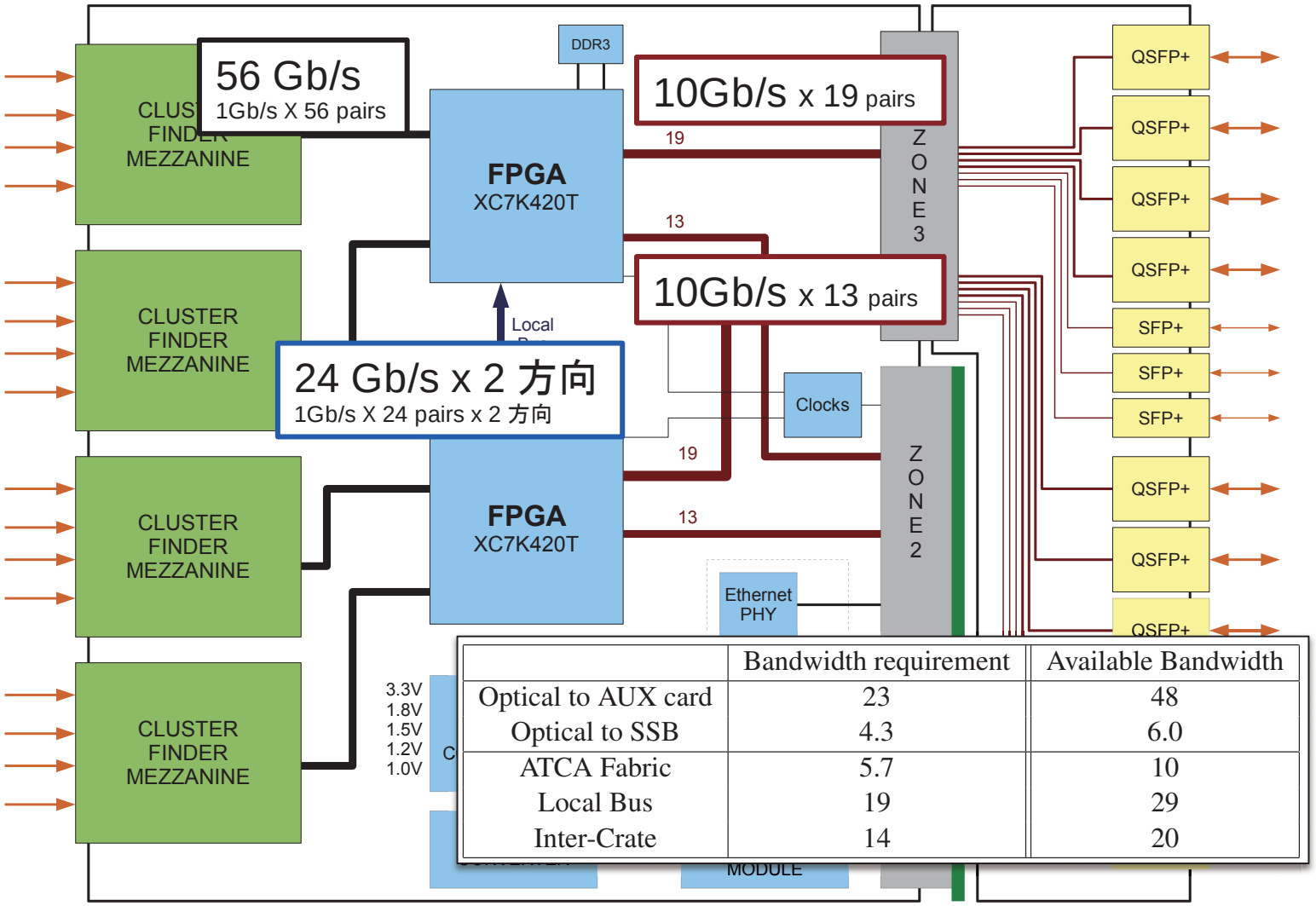
- *例 : ATLAS – FTK の Data Formatter System*
  - 4 ATCA クレート
  - 32 ボード
  - 64 FPGAs (Field Programmable Gate Array)



Data Formatter (pulsar IIa) Board

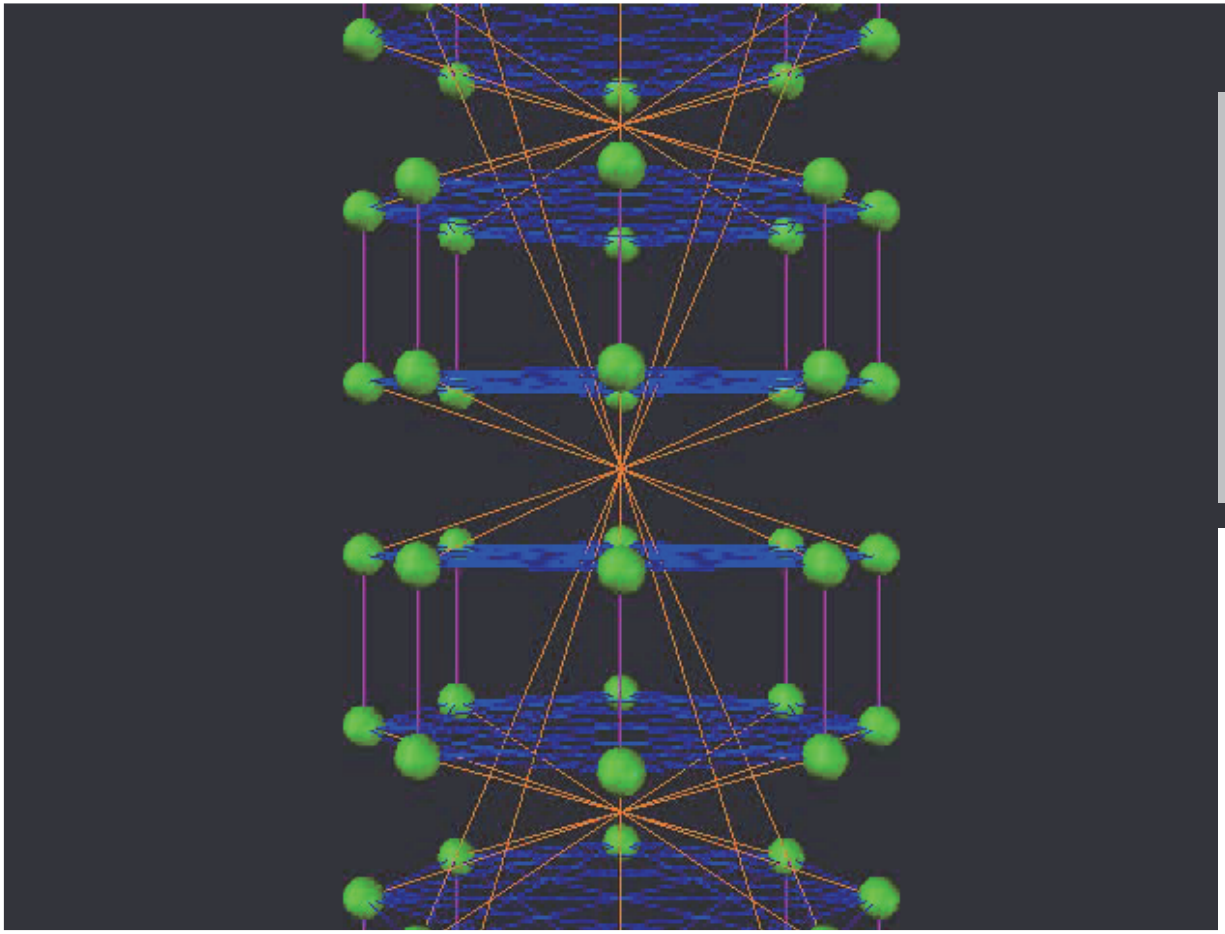


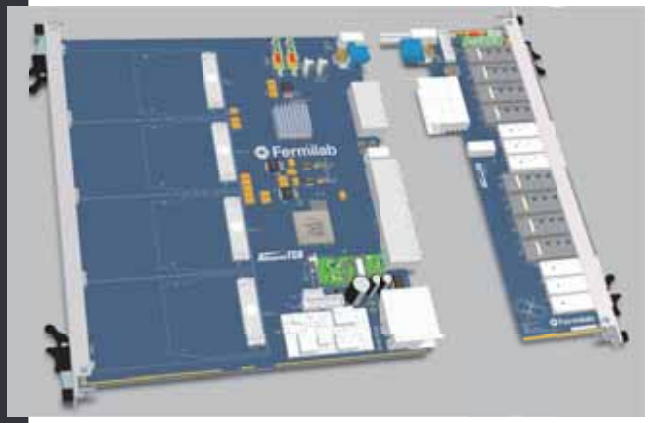
通信スピード

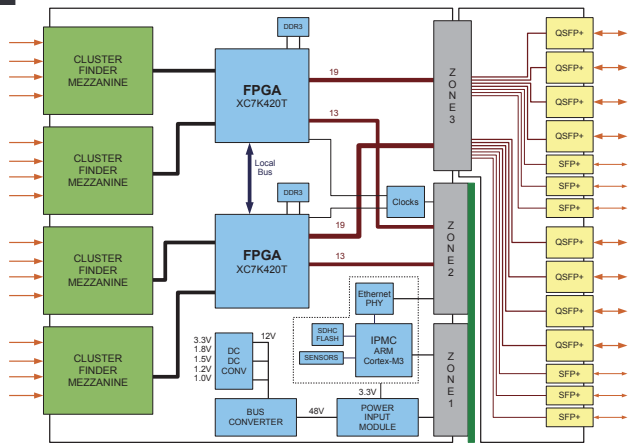


	Bandwidth requirement	Available Bandwidth
Optical to AUX card	23	48
Optical to SSB	4.3	6.0
ATCA Fabric	5.7	10
Local Bus	19	29
Inter-Crate	14	20

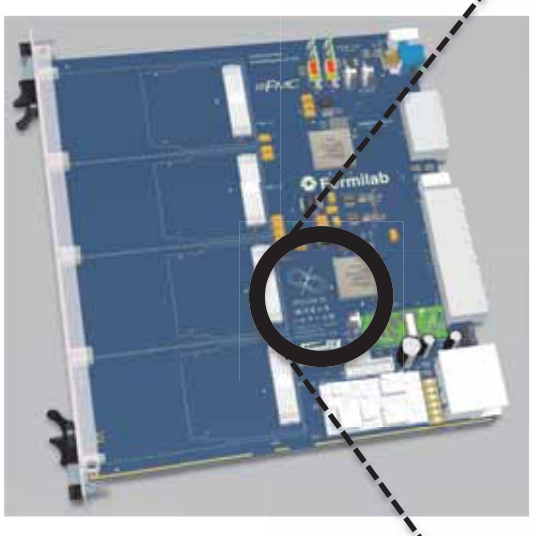
Data Sharing のトポロジー







おまけ


Fermilab


FMC1_1
PULSAR IIa
脈沖星二号
パルサーII型
J.Olsen / T.Liu / Y.Okumura
28 November 2012
PPD/EED Drawing 173843
U9
U21
C128
C127
AdvancedTCA

3D CAM

VIPRAM project (@ Fermilab)

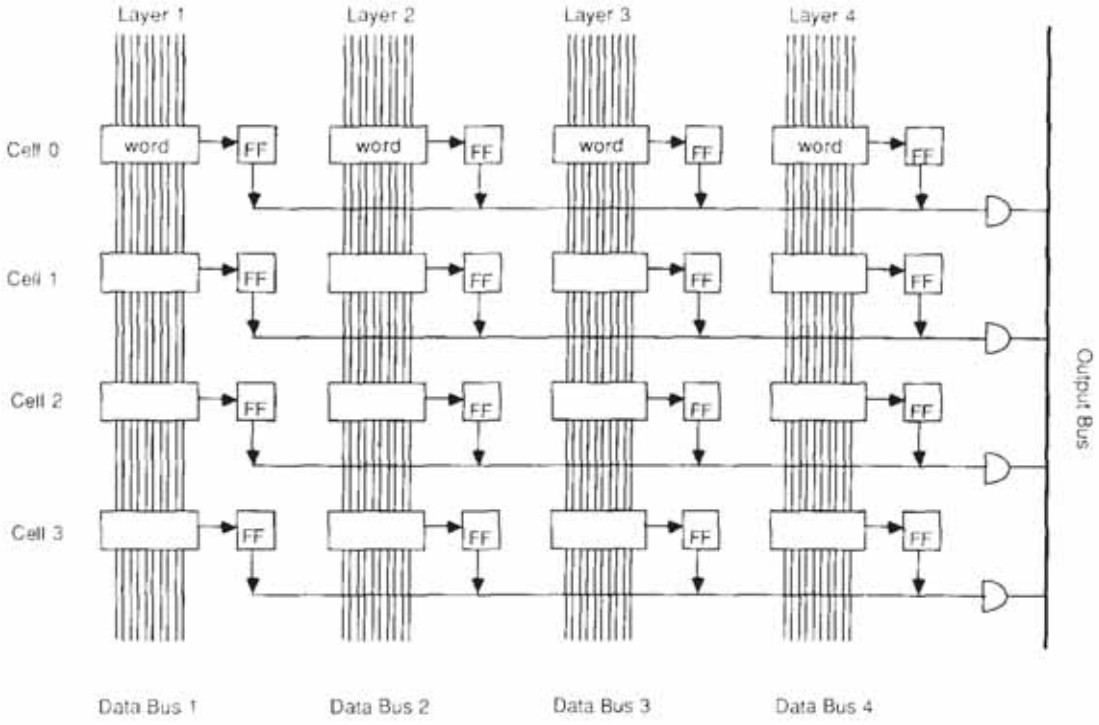
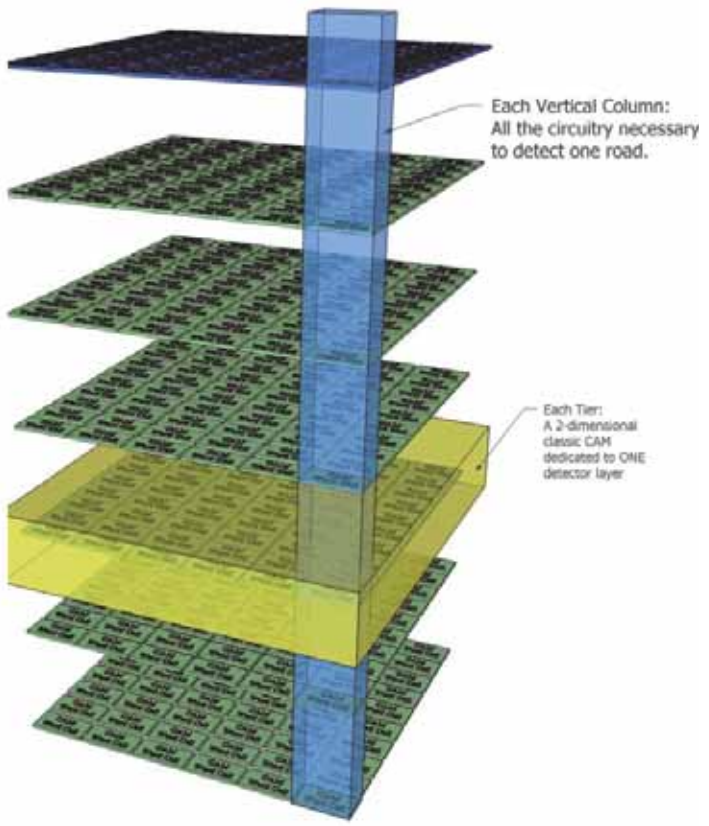
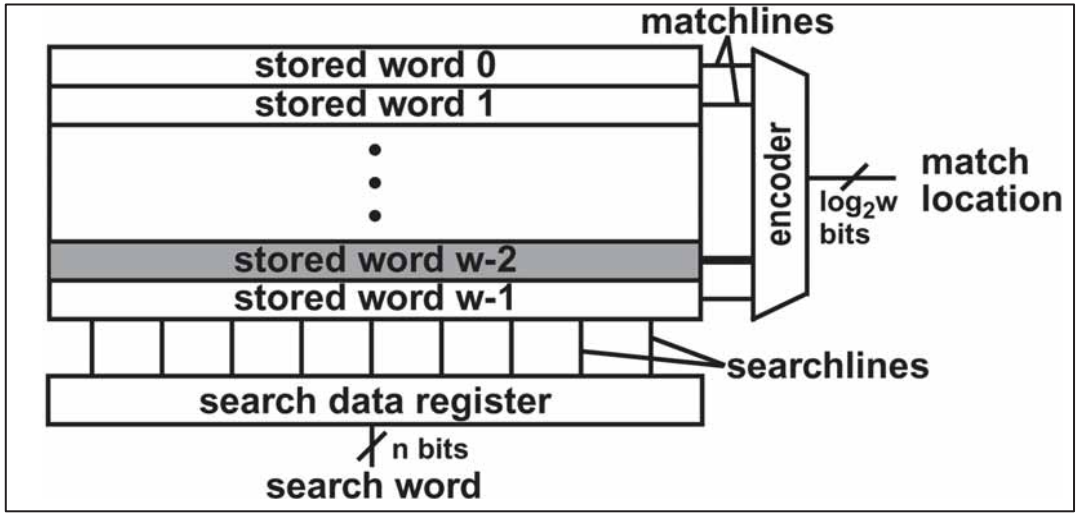


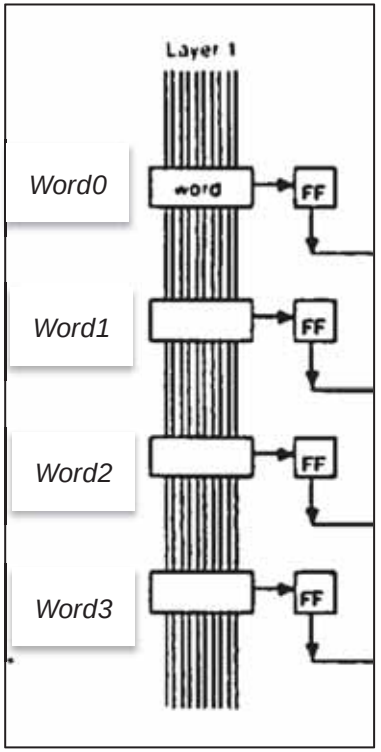
Fig. 3. Associative memory architecture.



CAM

- *Contents Addressable Memory (連想メモリ)*
  - 1) データを保存し、2) 入力データとの比較を行うメモリ
  - Network Router 等で用いられる技術



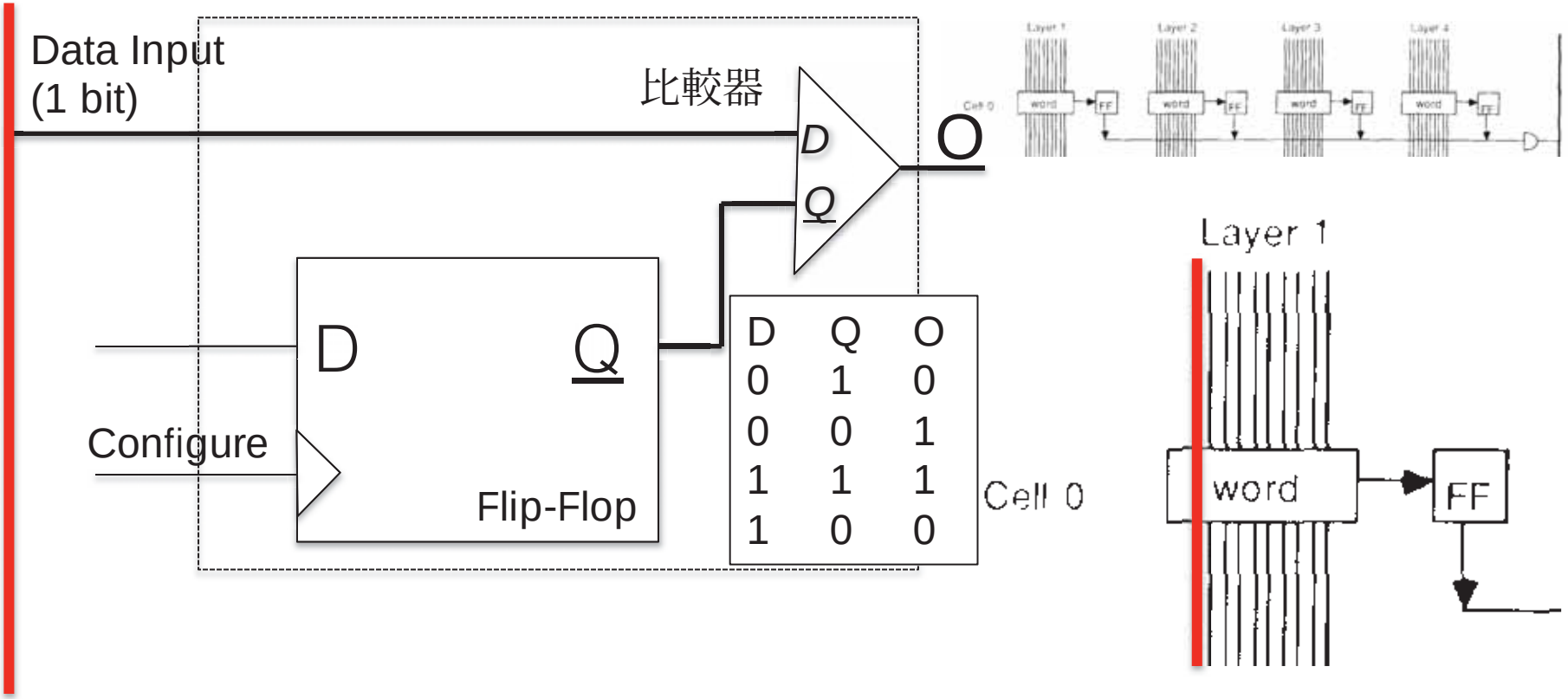


  - CAM を構成する回路コンポーネント
    - CAM-bit, CAM-CELL
    - 組み合わせで構成される Associative Memory

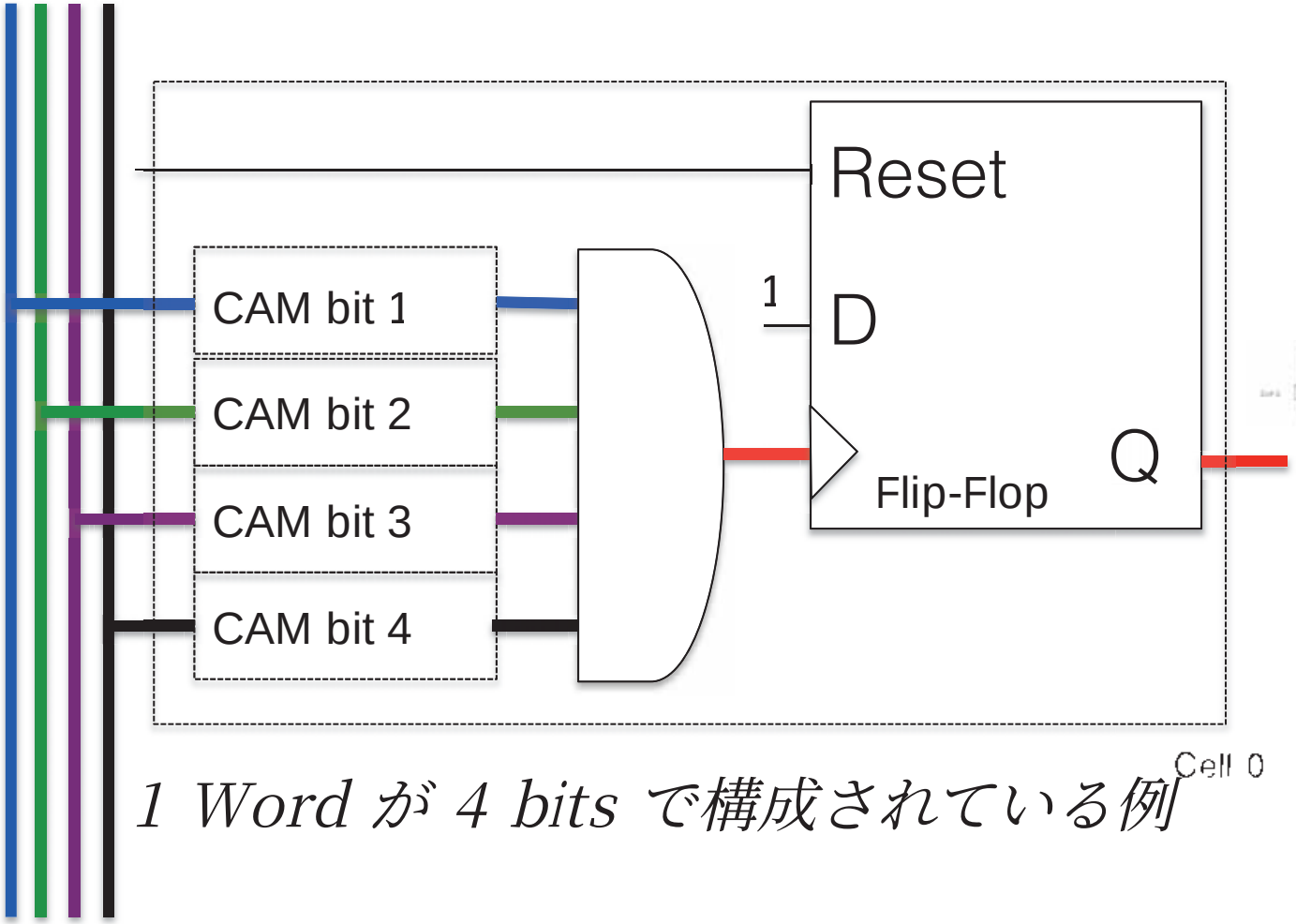
CAM bit 構造

Word の内の 1 bit を比較するための構成要素

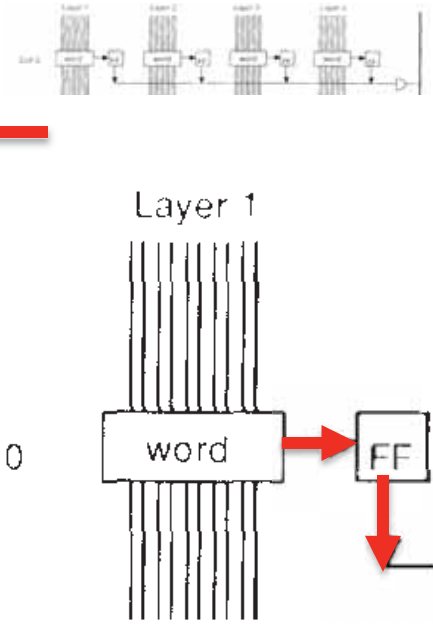
- Flip Flop
- 比較器



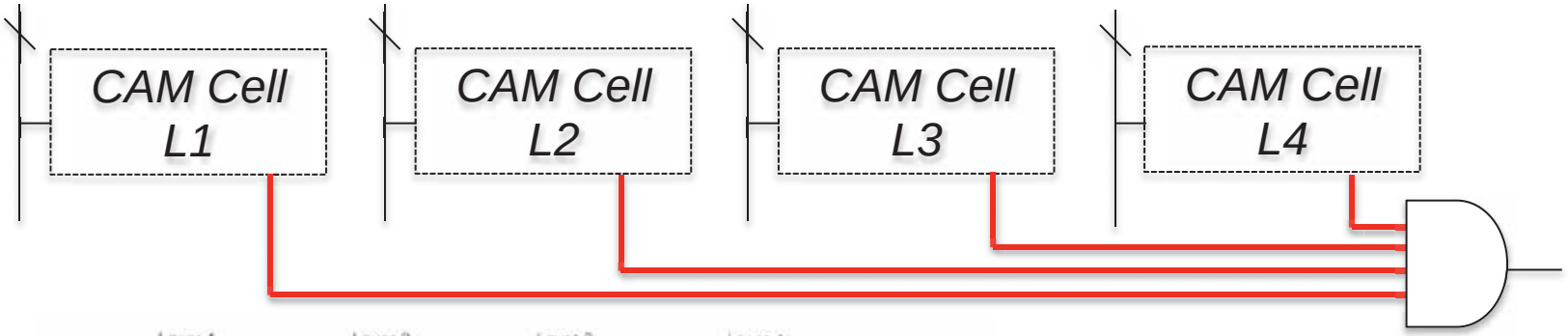
CAM Cell 構造



1 Word が 4 bits で構成されている例



CAM Cell の Majority Logic



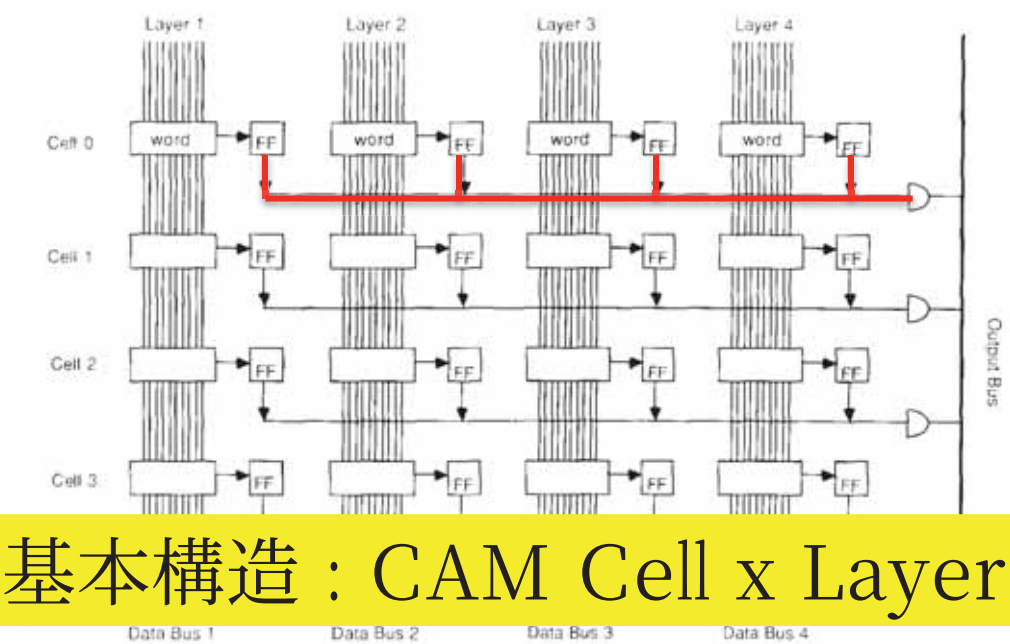
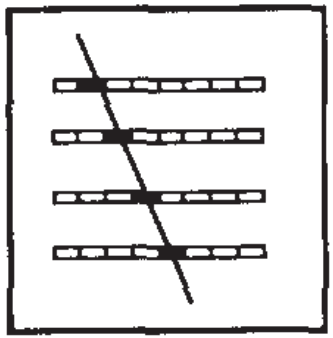


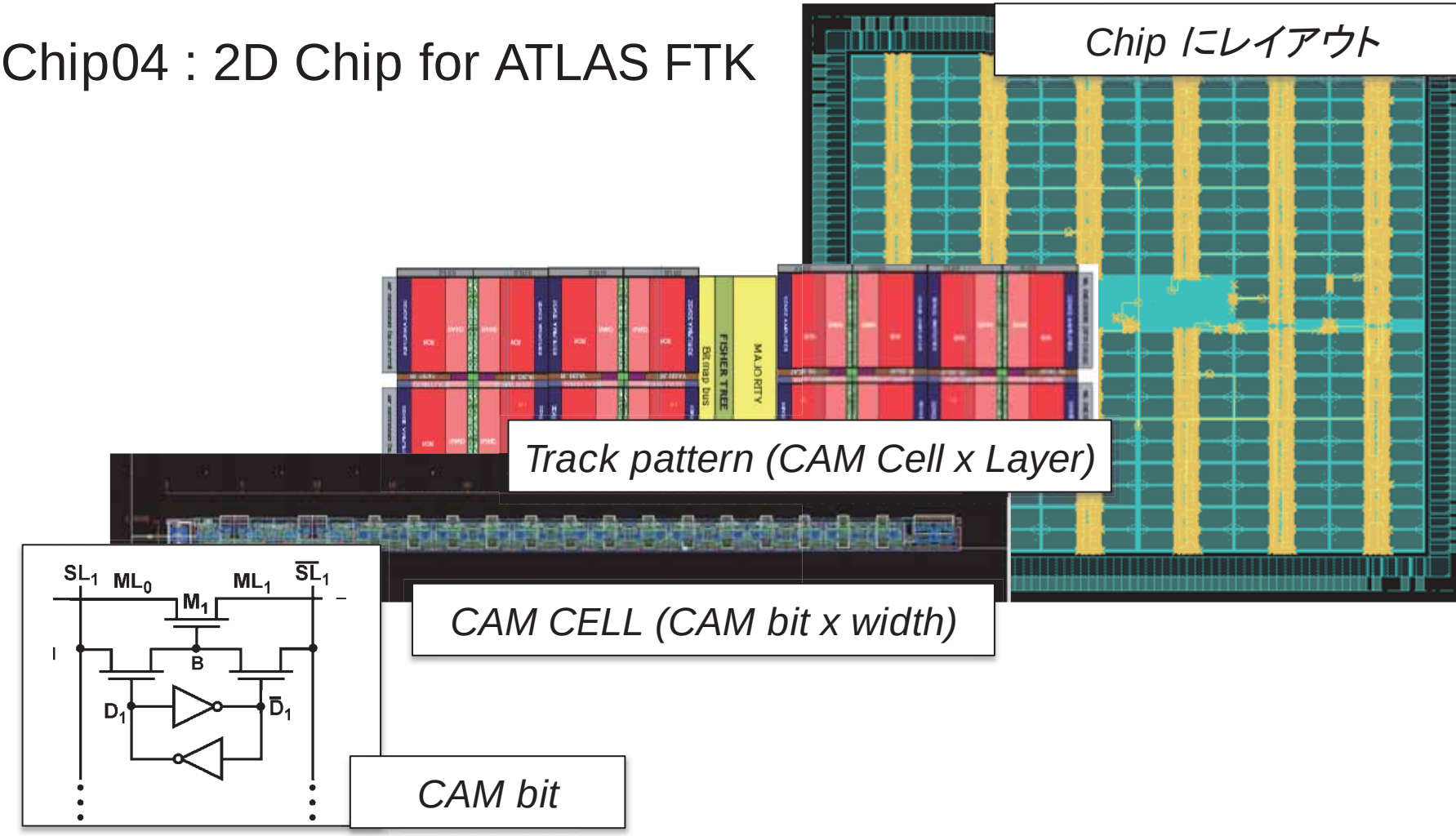
Fig. 3. Associative memory architecture.



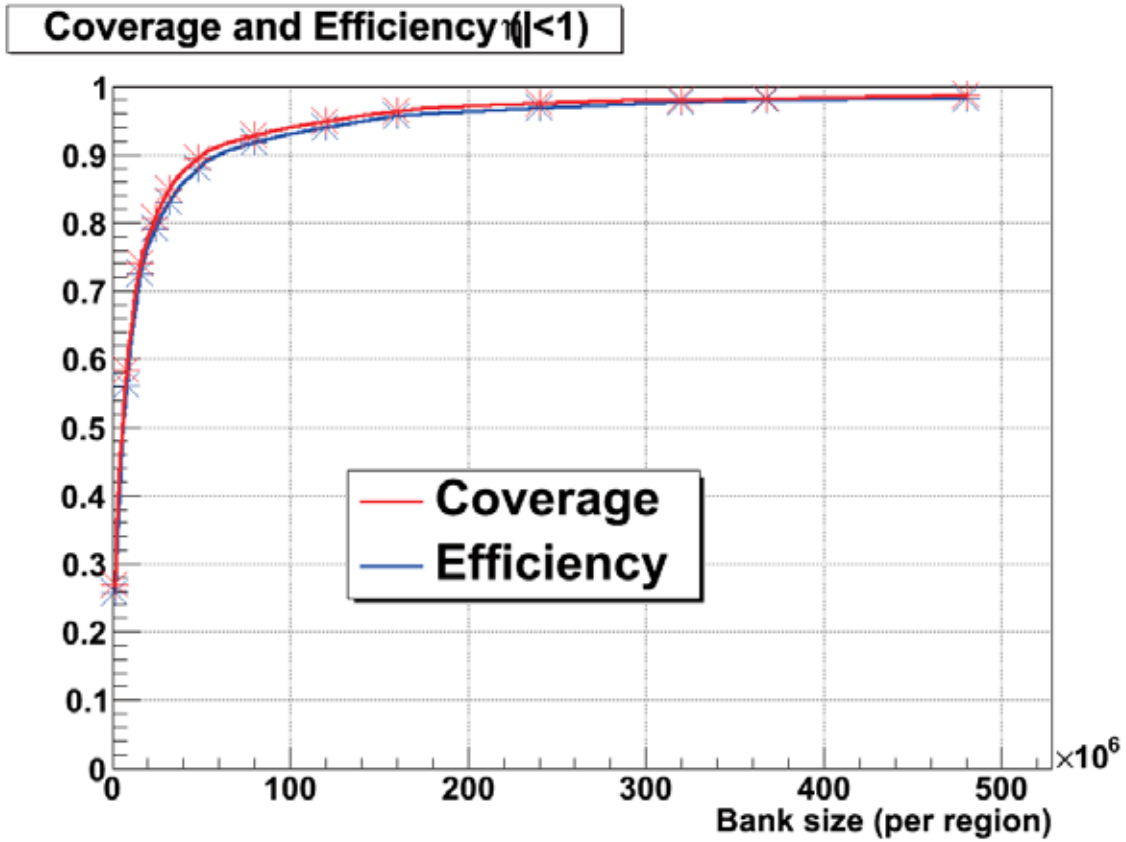
基本構造：CAM Cell x Layer 数 + AND = Track

2D チップ化 (AMChip04)

AMChip04 : 2D Chip for ATLAS FTK



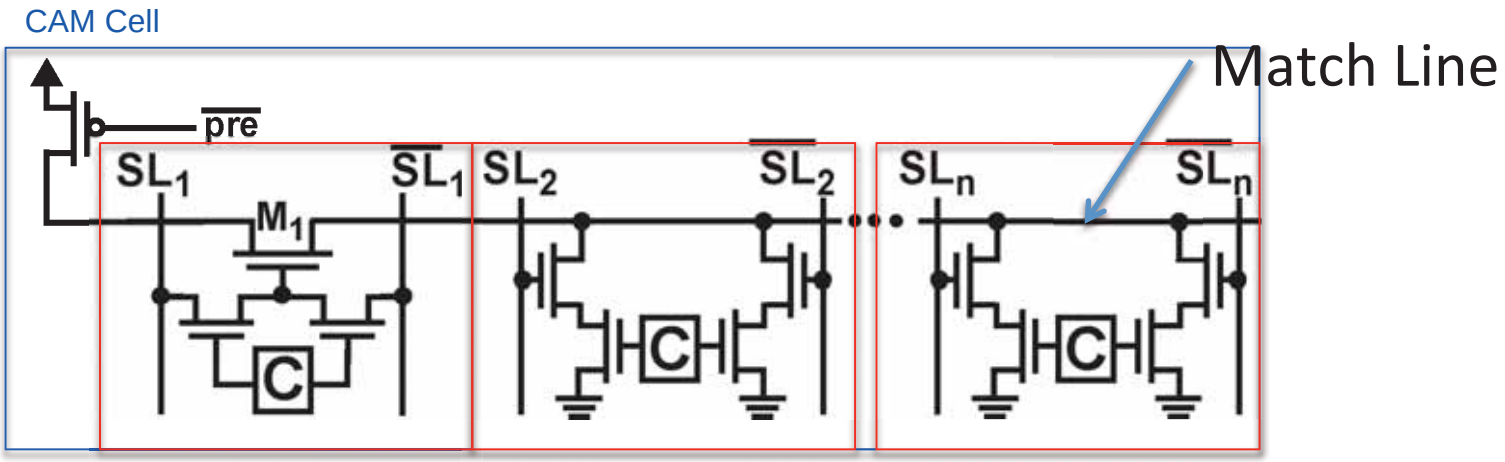
AM pattern vs Performance



集積度 (=構成要素のサイズ) が重要

AM チップ集積度 (1)

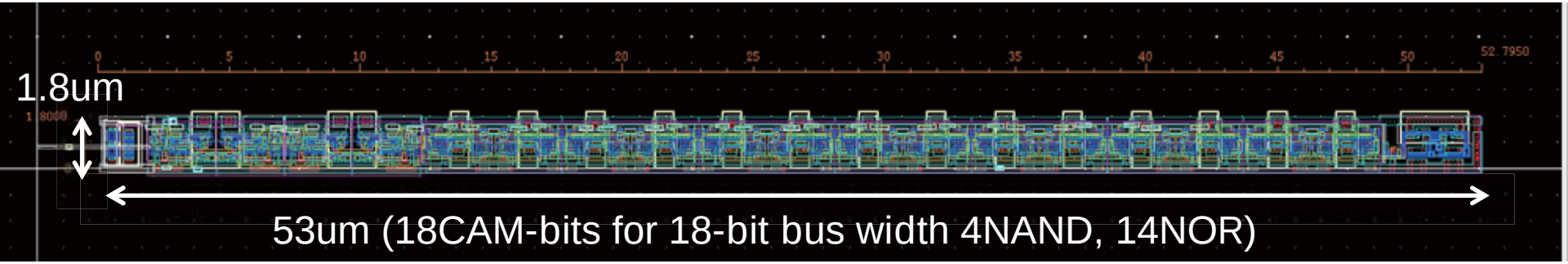
CAM Cell サイズ = 1.8 x 53 um^2



"NAND" CAM bit
(2.6um x 1.8um)

"NOR" CAM bit
(2.6um x 1.8um)

65nm CMOS で実装

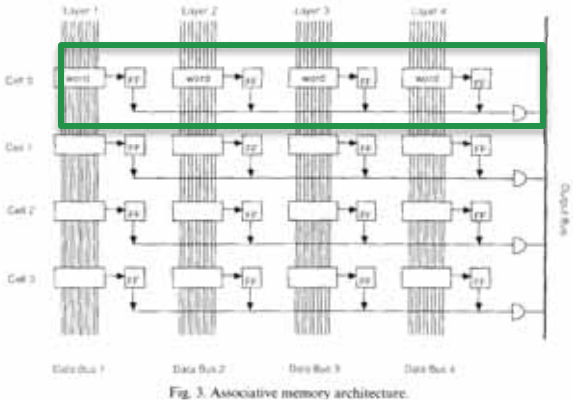


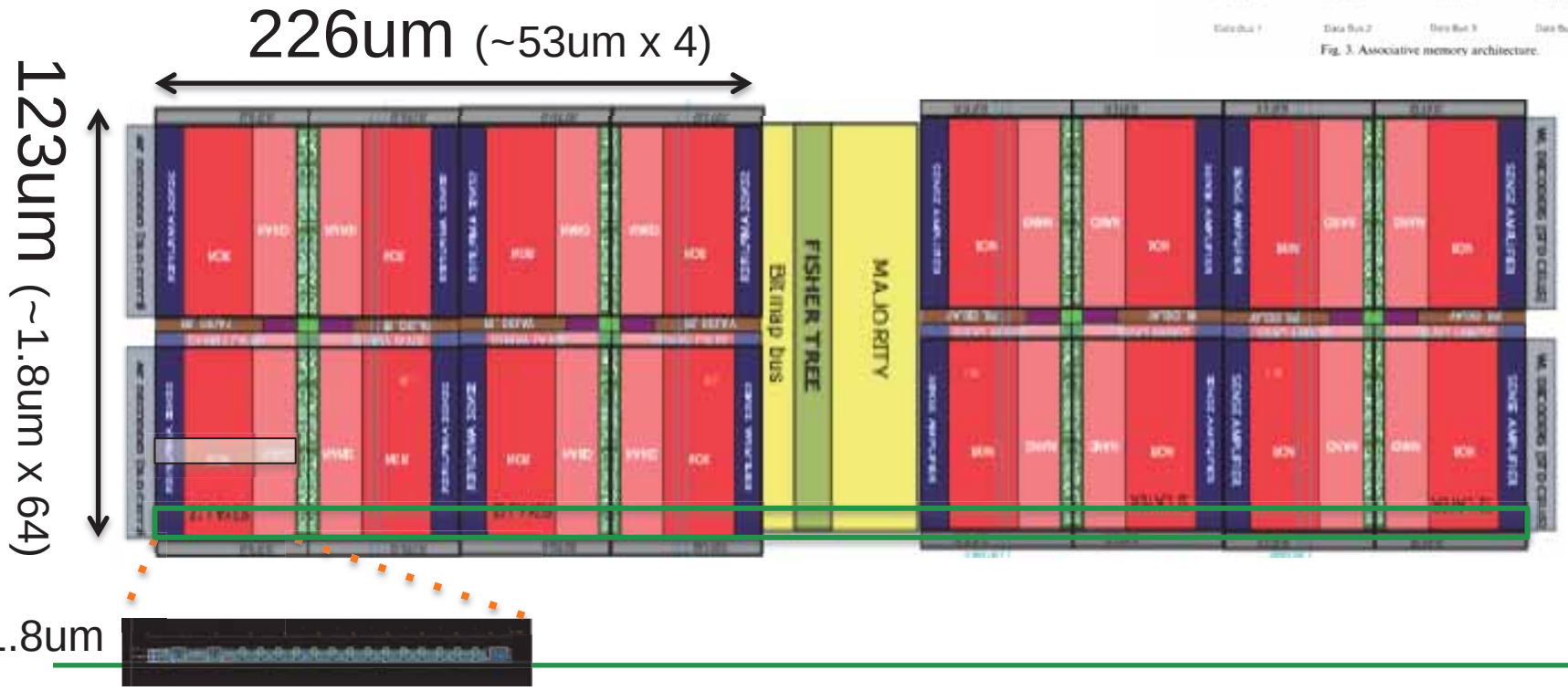
AM チップ集積度 (2)

8 Layer トラックパターン

(Pixel x 3, SCT x 5 で Track Finding)

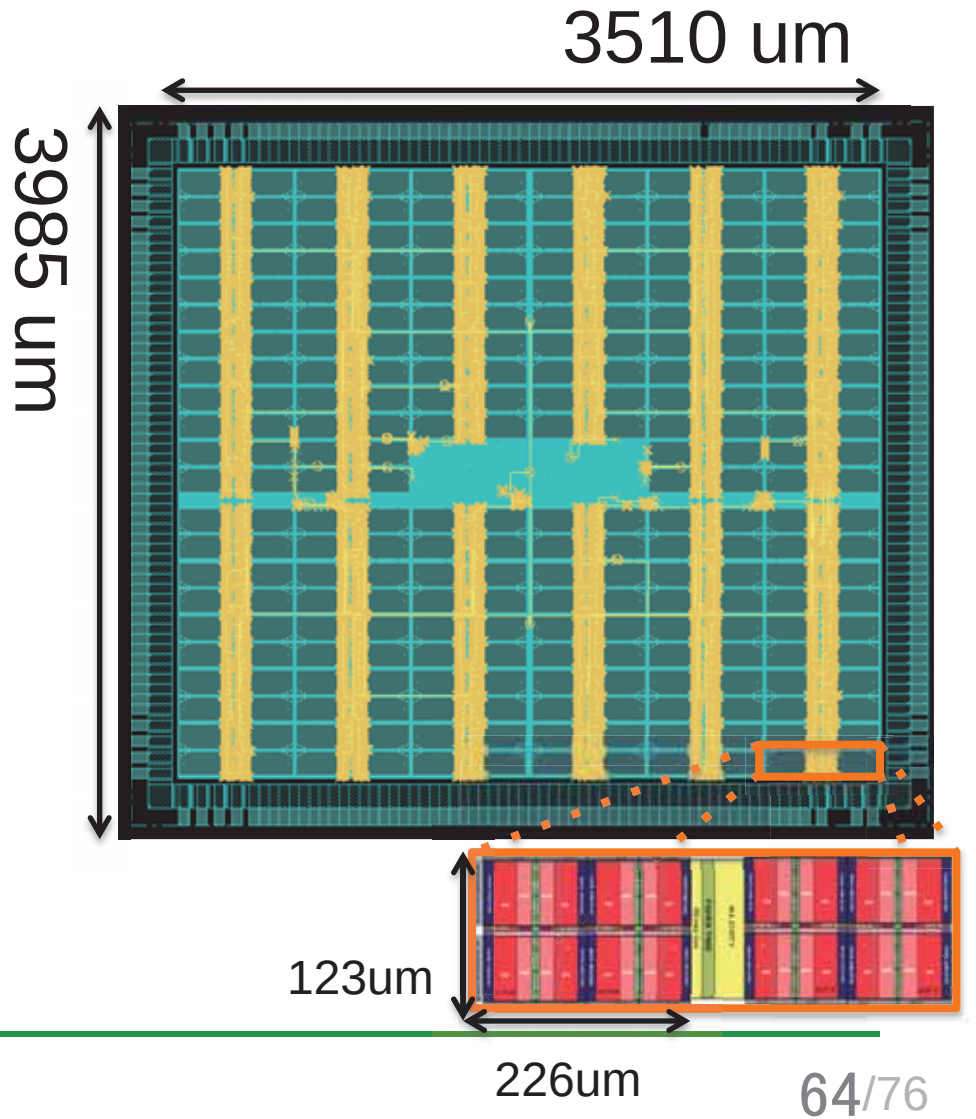
8 CAM Cell + Majority Logic = Track Pattern



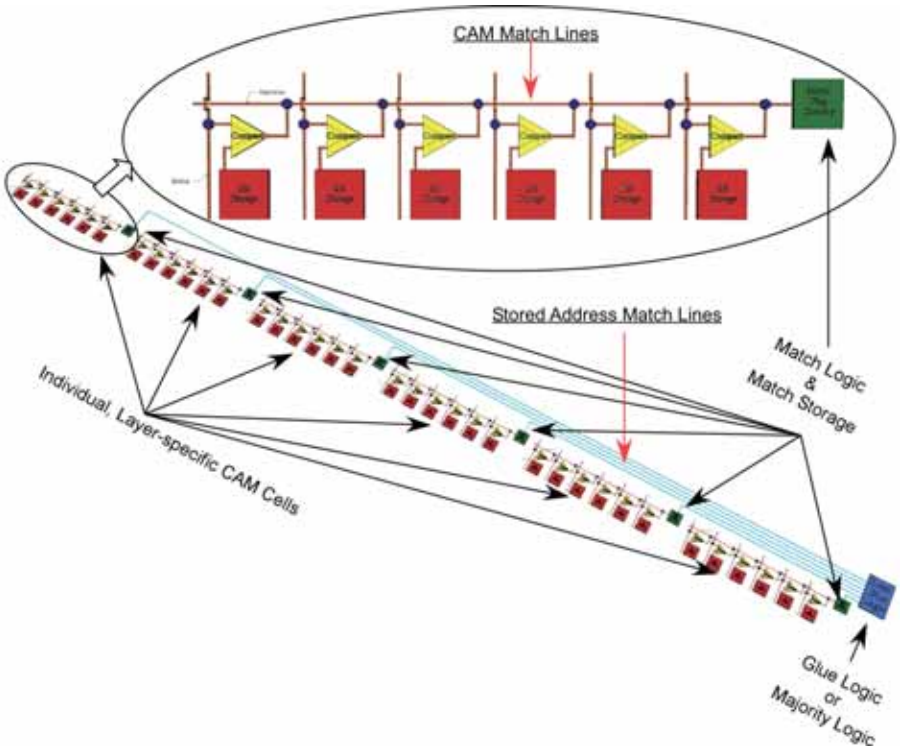


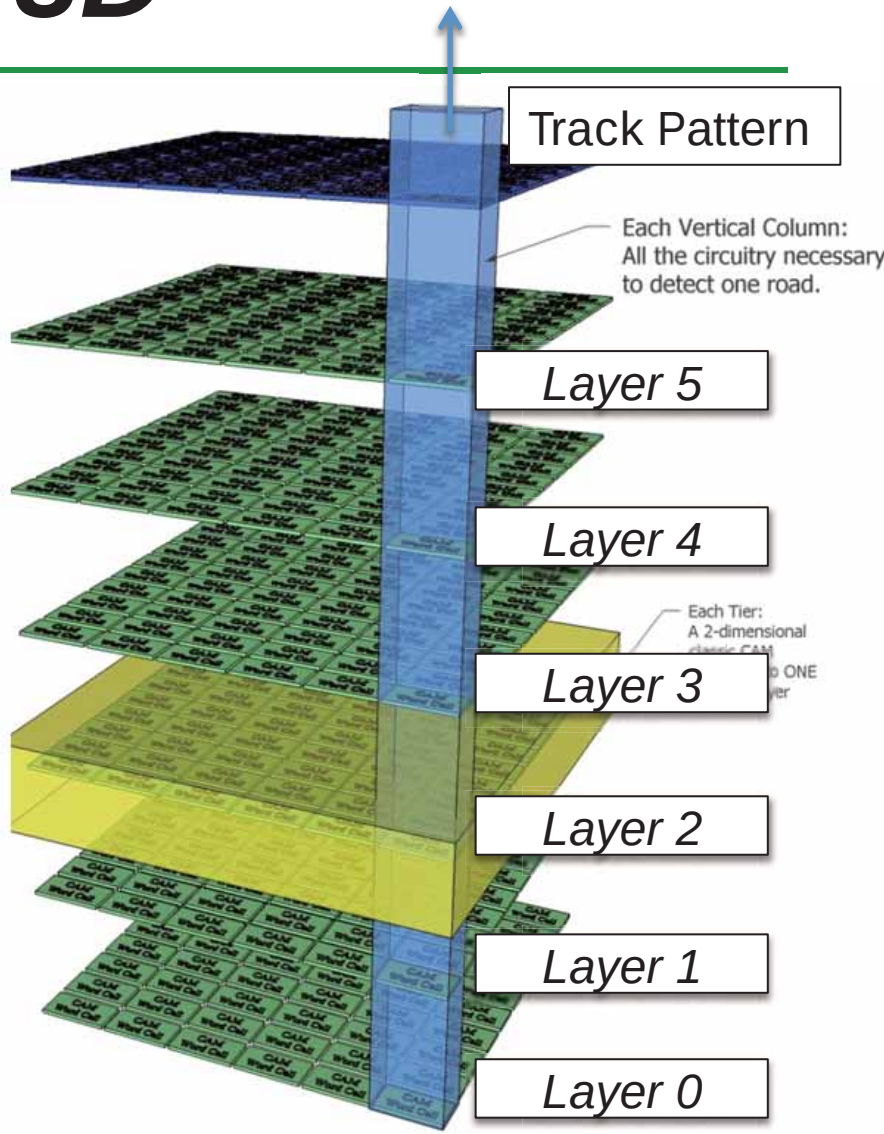
AM Chip 集積度 (3)

- *AMChip04 prototype (for ATLAS FTK)*
  - 128 blocks
  - 128 x 64 tracks = 8k
  - 2 W @ 100 MHz
- *Production Type*
  - 12mm x 12mm
  - 80k tracks



2D → 3D

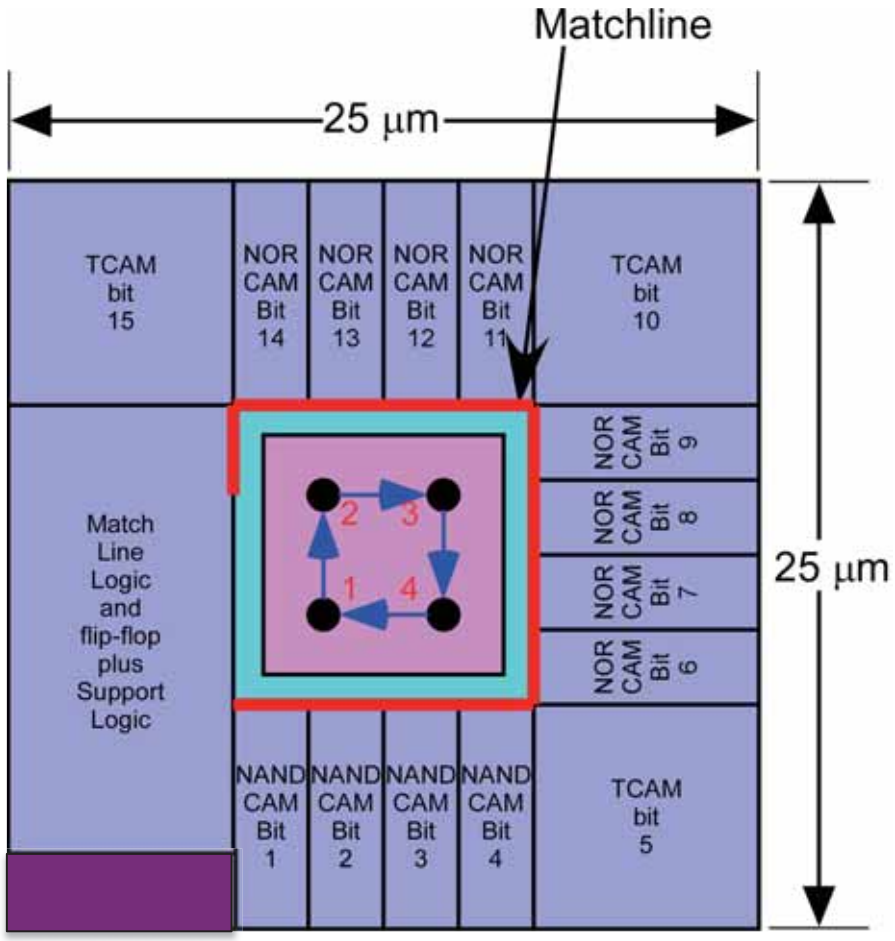




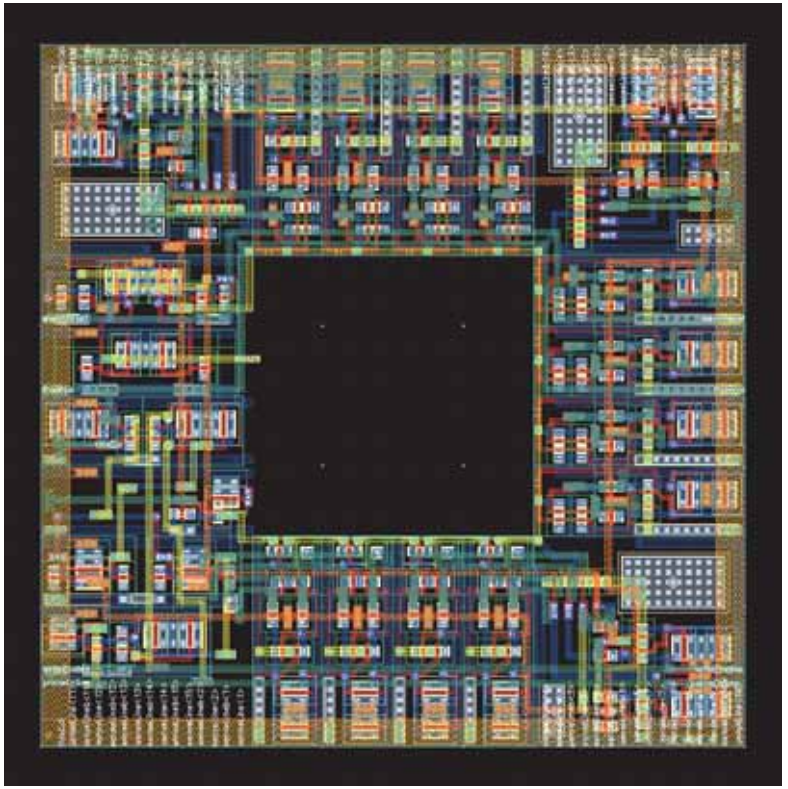
3 次元化のご利益

- ✓ Track Pattern (高集積)
- ✓ Layer 間の経路長が短くなる
  (高速化 or 低電力化)

3D 仕様の CAM Cell

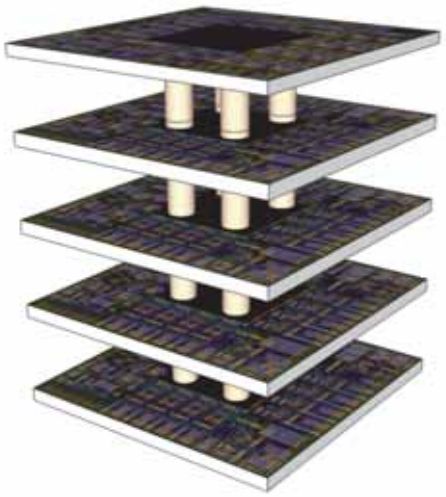


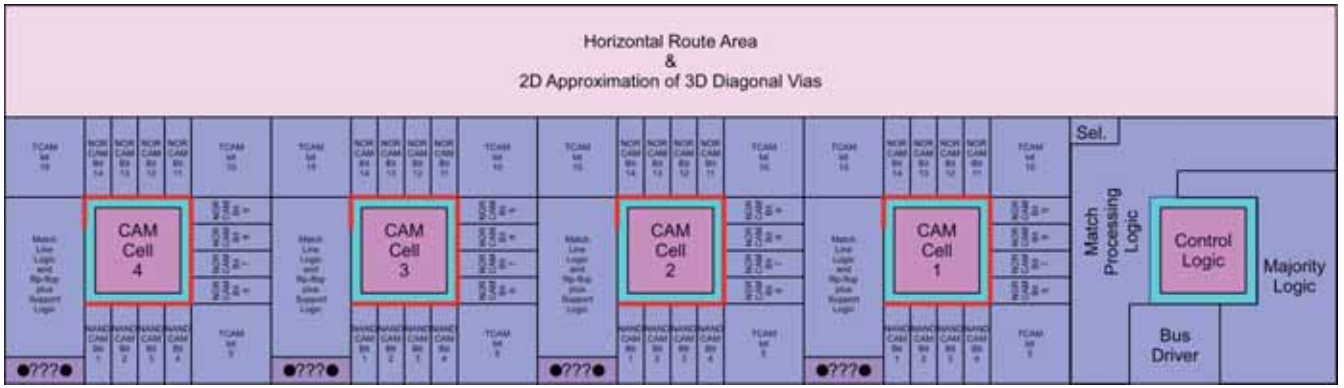
参考 For 2D



130nm Global Foundries Low Power CMOS

3D へ向けた 2D の proto type



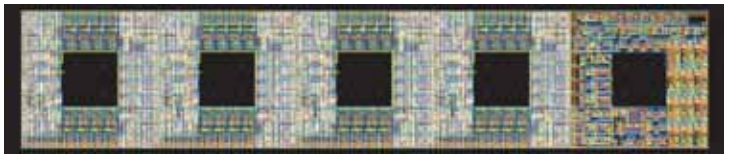


130nm Global Foundries Low Power CMOS

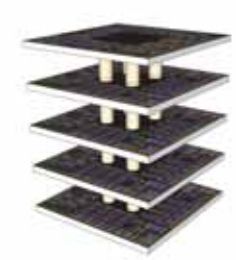
- ✓ 25um x 125um
  CAM Cells (4 Layer) + 1 Majority Logic

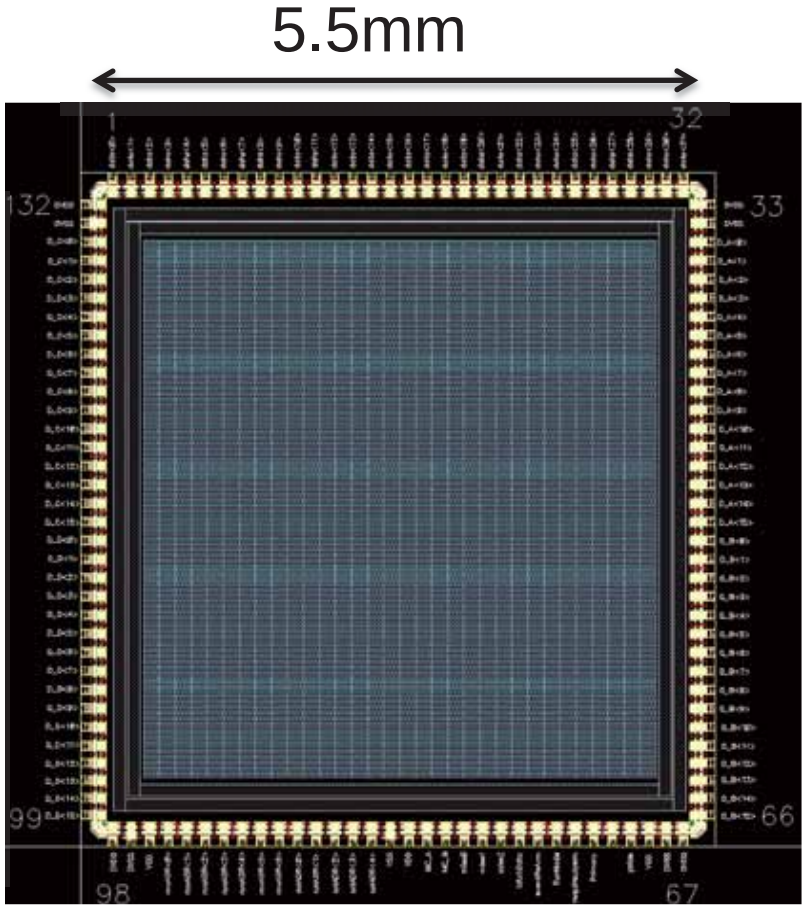
プロトタイプ

- *3D 化用の CAM Cell を実装*
  - 5.5mm x 5.5mm
  - 約 50000 Cells
  - 10k track patterns (4-layer track)



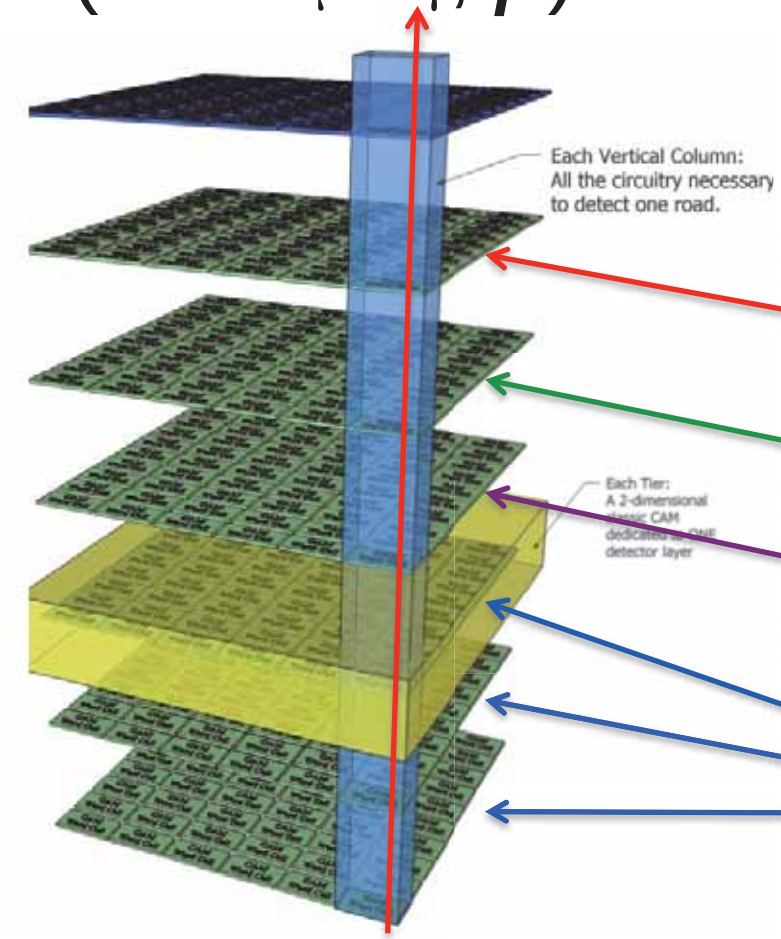
  - 3 D 化すると、50k track patterns (しかも省エネ)





こんなこともトリガーでできる？

(PID e/μ/h/γ, ***p***)

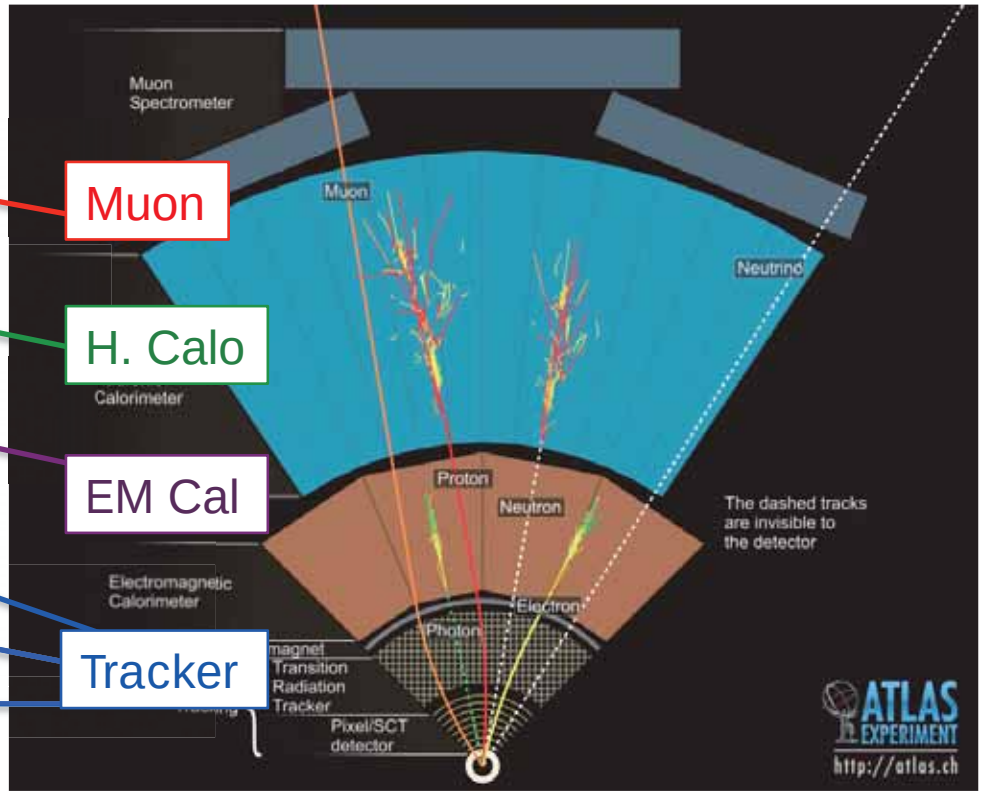


Muon

H. Calo

EM Cal

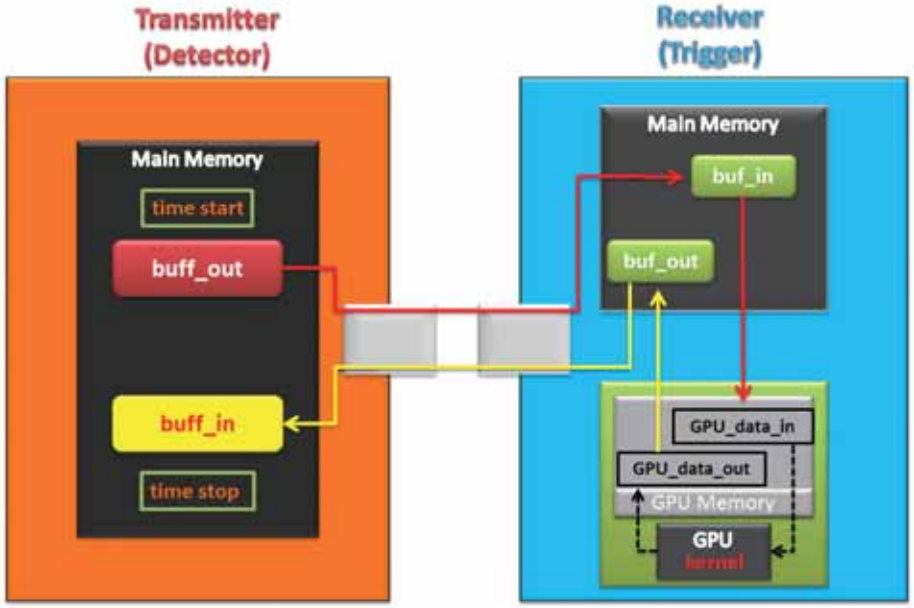
Tracker

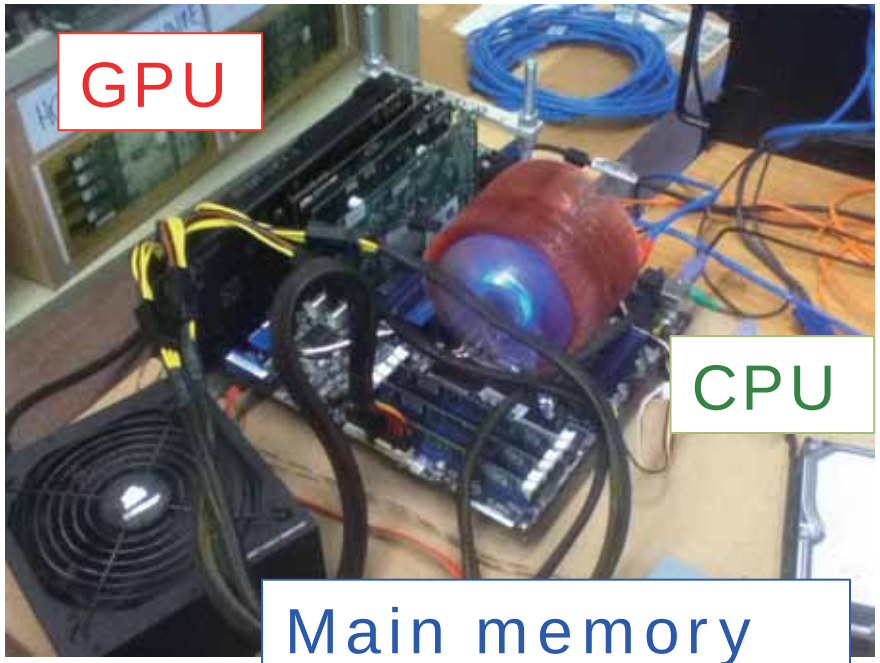


Graphical Processing Unit の Tracking への応用

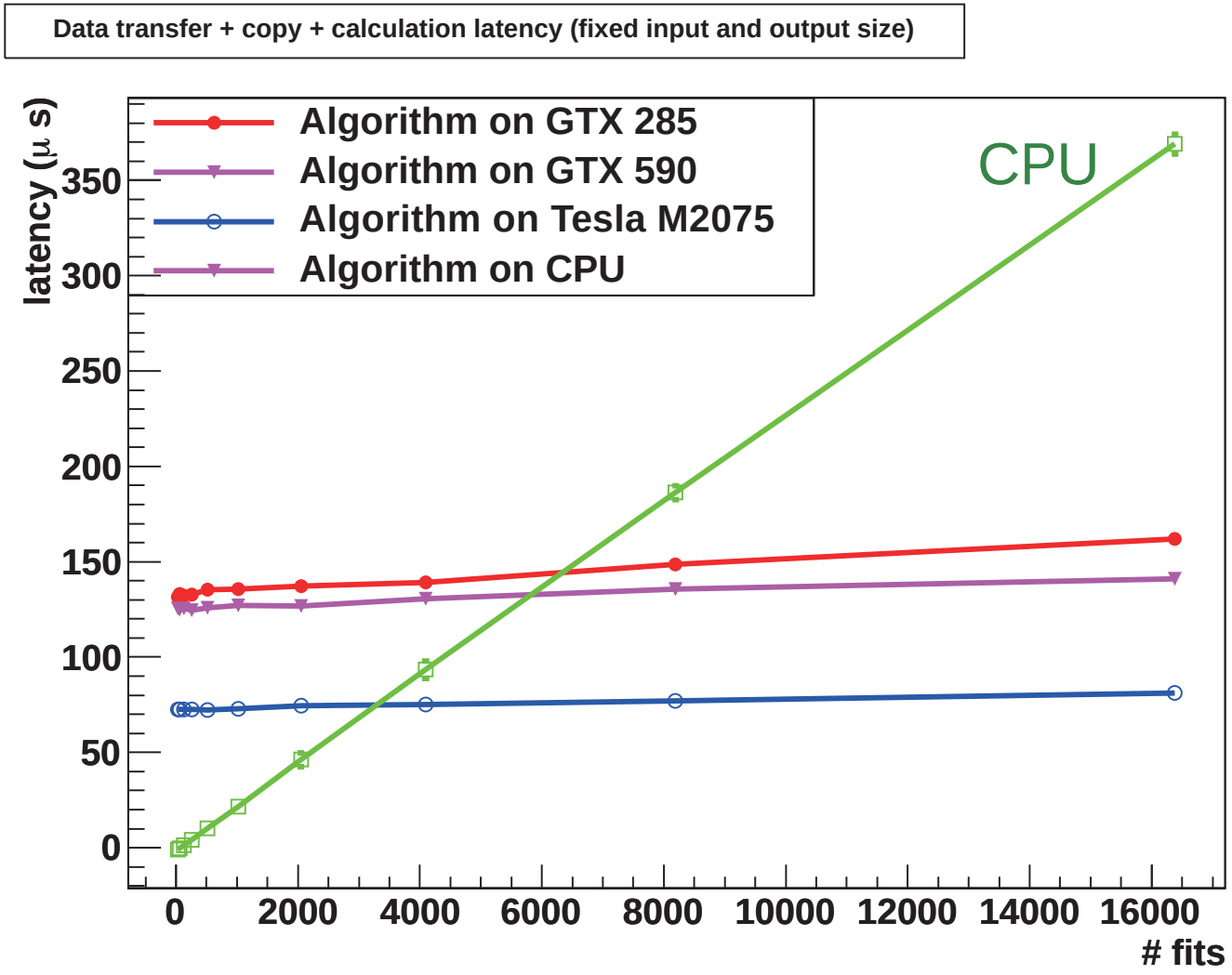
GPU for Track Fitting

- *Graphical Processing Unit (GPU) の特徴*
  - 並列処理 (マルチスレッド) が得意
    - 特に同じ処理を何度も何度も独立に繰り返すような処理が得意
  - 複数のトラックフィッティングを並列処理可能性



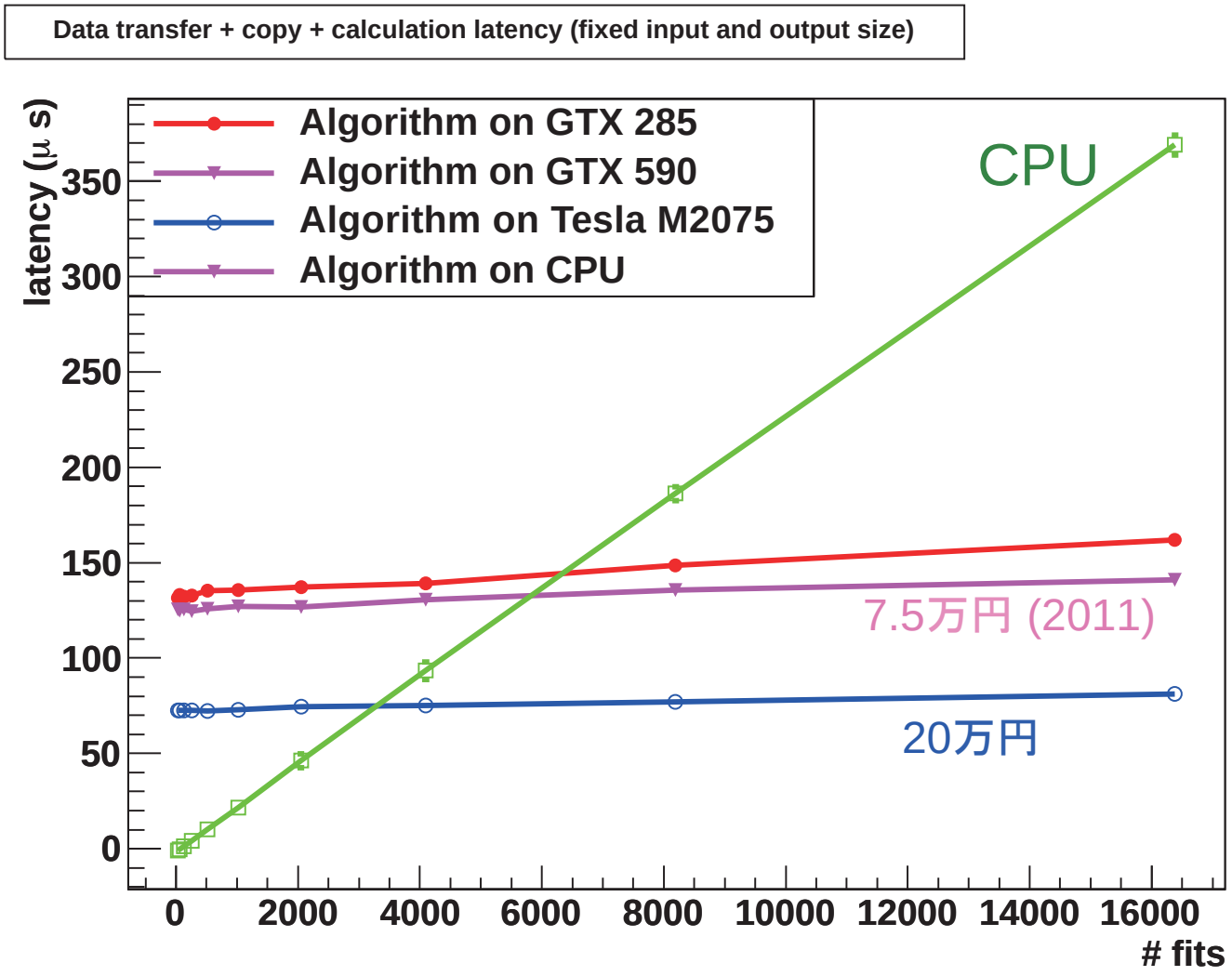


Track Fitting Speed



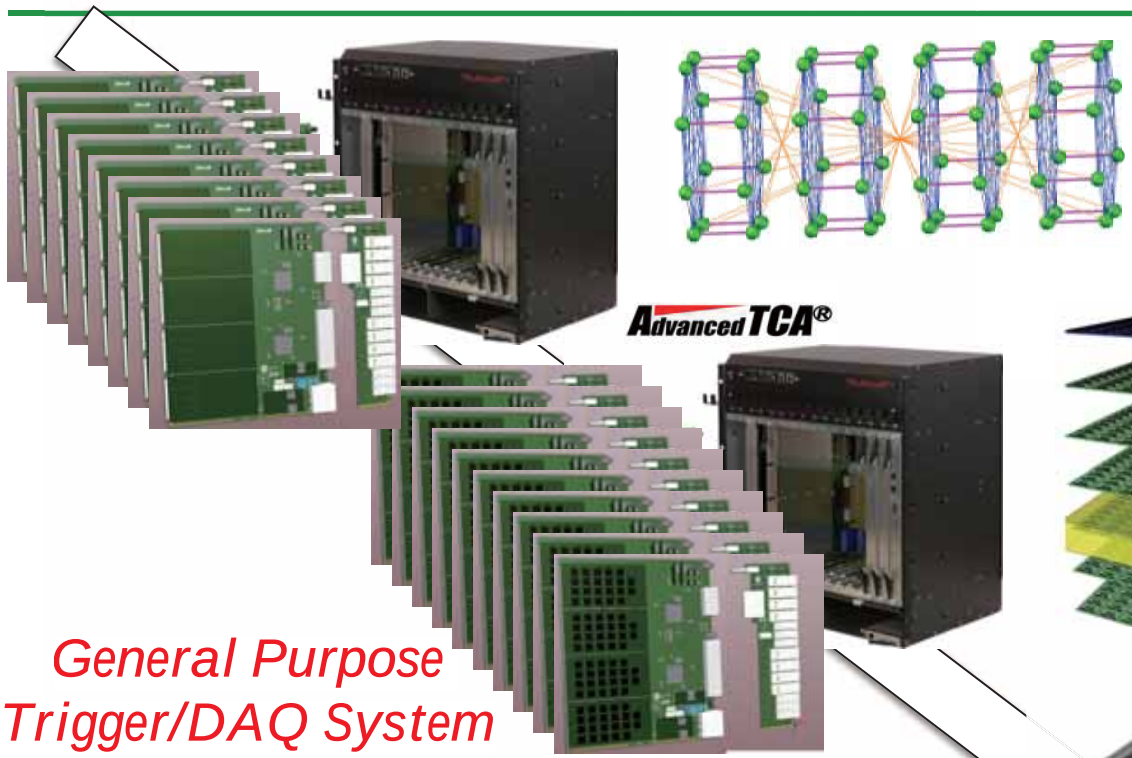
~1ns/fit の処理が一つの GPU で可能 (I/O offset は除く)

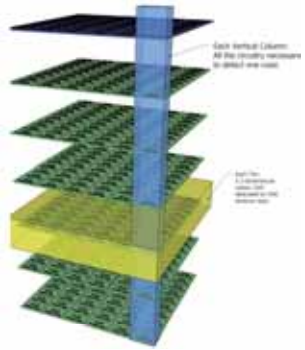
Track Fitting Speed



~1ns/fit の処理が一つの GPU で可能 (I/O offset は除く)

General Purpose TDAQ





GPU farm

General Purpose Trigger/DAQ System with MASSIVE parallel processing & pattern recognition power

Patterns ~ Billion / shelf

まとめ

高速飛跡検出の実現の意義

$L=3\times10^{24}/cm^2/s=10Hz/nb$の pp 衝突実験の実現

Associative Memory アプローチによる飛跡再構成

ATLAS 実験の (FastTraker) FTK システム

最新技術開発の紹介

ATCA, 3D CAM, GPU

応用も考え中。

何か思い付いた方は是非ご連絡ください。

おしまい